

ADC performance: time dependence

BNL DUNE

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BNL

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Introduction

I have been looking at ADC test data taken at BNL

- I report here on long-term data taken in March 2017
 - ADC samples are read out for input voltage steps with sawtooth envelope
 - 40M samples over 20s for each ADC channel
 - approximately 10k samples for each ADC bin
- Data is from new P1 chips for protoDUNE
- Data conditions
 - Cold (LN2)
 - There is warm data for one chip
 - 2 MHz sampling
 - All data taken with external clock
 - Single chip (D02) in board kept cold and powered
 - 18 samples taken over 10 days

Data taking

Data taken by the following team

- Hucheng Chen, Shanshan Gao, Jack Fried, Feng Liu (BNL)
- Damian Goeldi (Univ. of Bern)

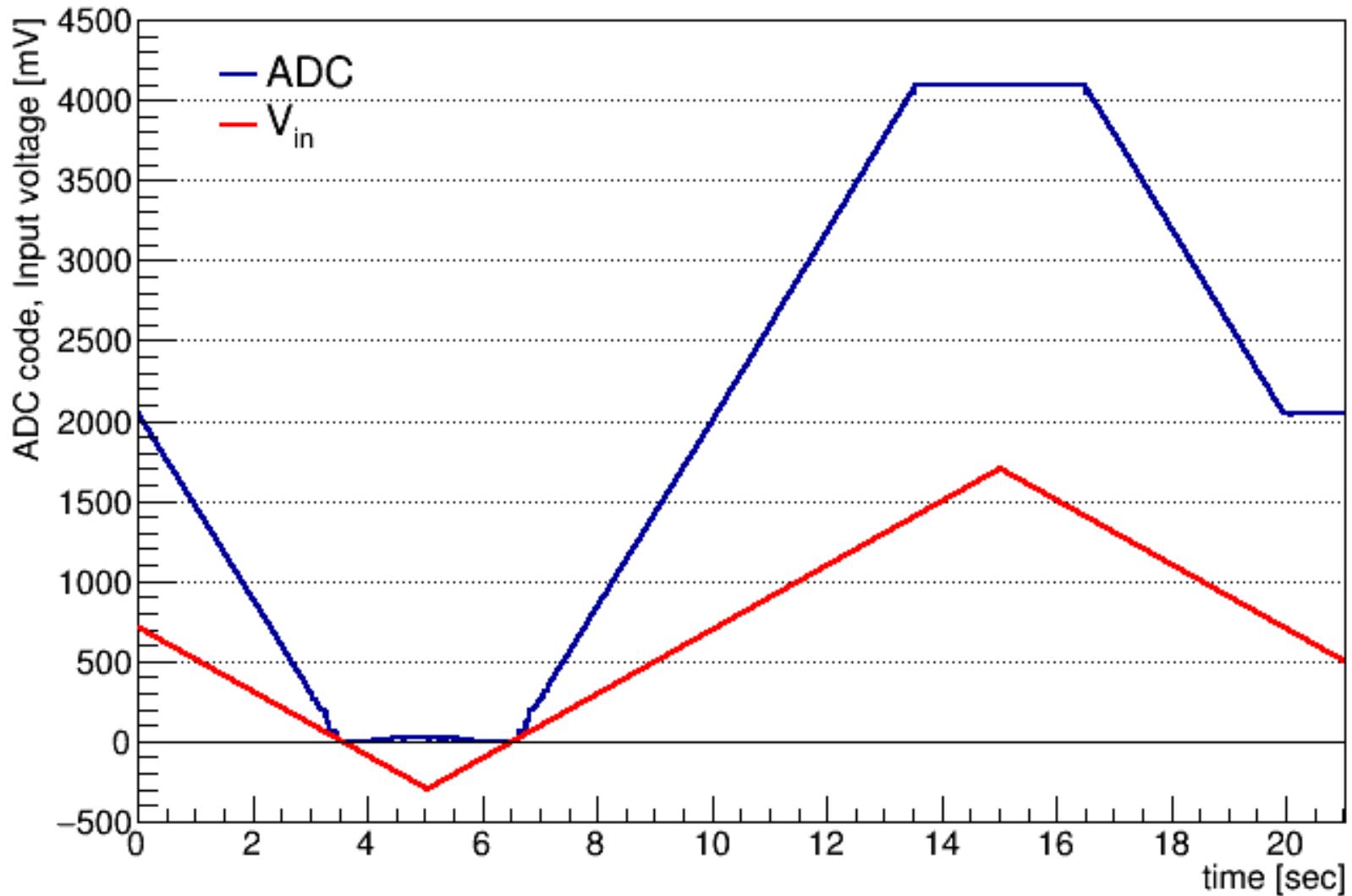
Thanks to them to making this data available to me

Data format

- ADC samples
- Input voltage ramp from –300 to 1700 mV at 200 mV/sec
- Data is approximately one period of sawtooth centered on the rise
 - See plot on following page
- I see ADC get stuck at a value near 2000 after 20 sec
 - See following example plot
 - I keep only the first 19.8 sec of data for each sample
 - Waveform plots show all samples then look OK

Example waveform

201703b_D02_6b channel 4



Data analysis

Data is analyzed as described in previous talks

- Also see appendix

First need input voltage

- This was provided by data takers for earlier samples
 - Those were in CSV format with one rise starting at a specified voltage
- Here data is ADC only (channel number packed in high bits)
 - Known waveform: sawtooth with 10 s rise/fall over (-300, 1700) mV
 - But time offset is not specified
- I determine the min and max points from ADC data in two ways
 - Data above or below a double threshold
 - Midpoints between peaks in the ADC bin distributions
 - Require these to agree with one another
- Assume the min and max found in this way correspond to the same for the input voltage → timing offset and period
- Preceding plot shows V_{in} determined in this way

Results

Performance plots are in appendix

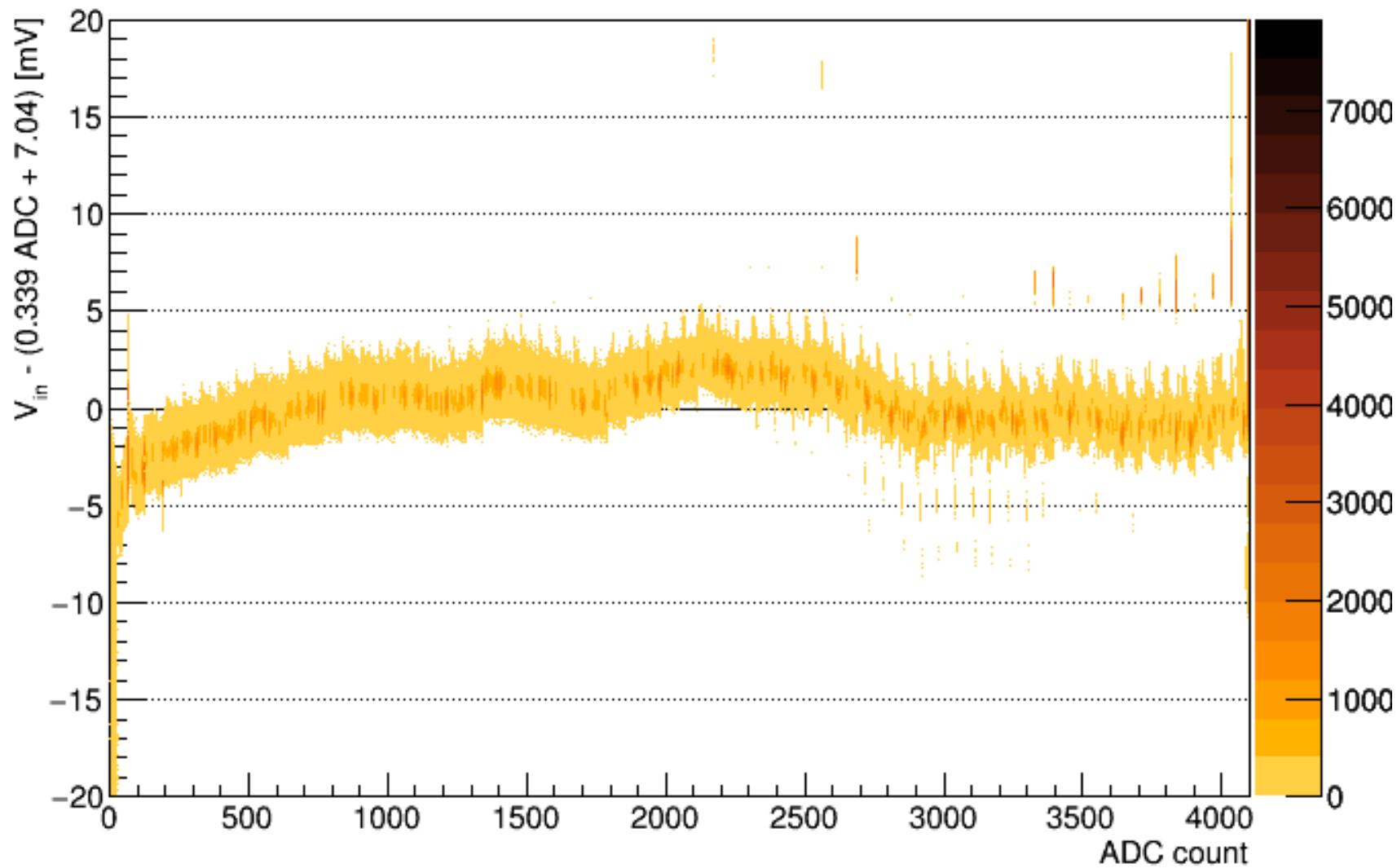
- 18 samples for one chip
- Taken over 10 days

Comments

- Bulk response seems very consistent day-to-day
 - Overall gain RMS is 3.6% (primarily channel-to-channel variation)
 - Largest gain RMS for any one channel is 0.03%
 - No bulk changes evident in residual spectra
- There is some change in the bad channels and tails
 - Many the same day after day but some appear or disappear
 - Biggest changes in channel 6—plots on following pages
 - Many plots for all channels and times in appendix 2
- Work in progress to quantify these changes
 - E.g. what are bad and tail fractions if we combine all samples or take the worst of each?
 - Effect of using the “wrong” sample to identify problems

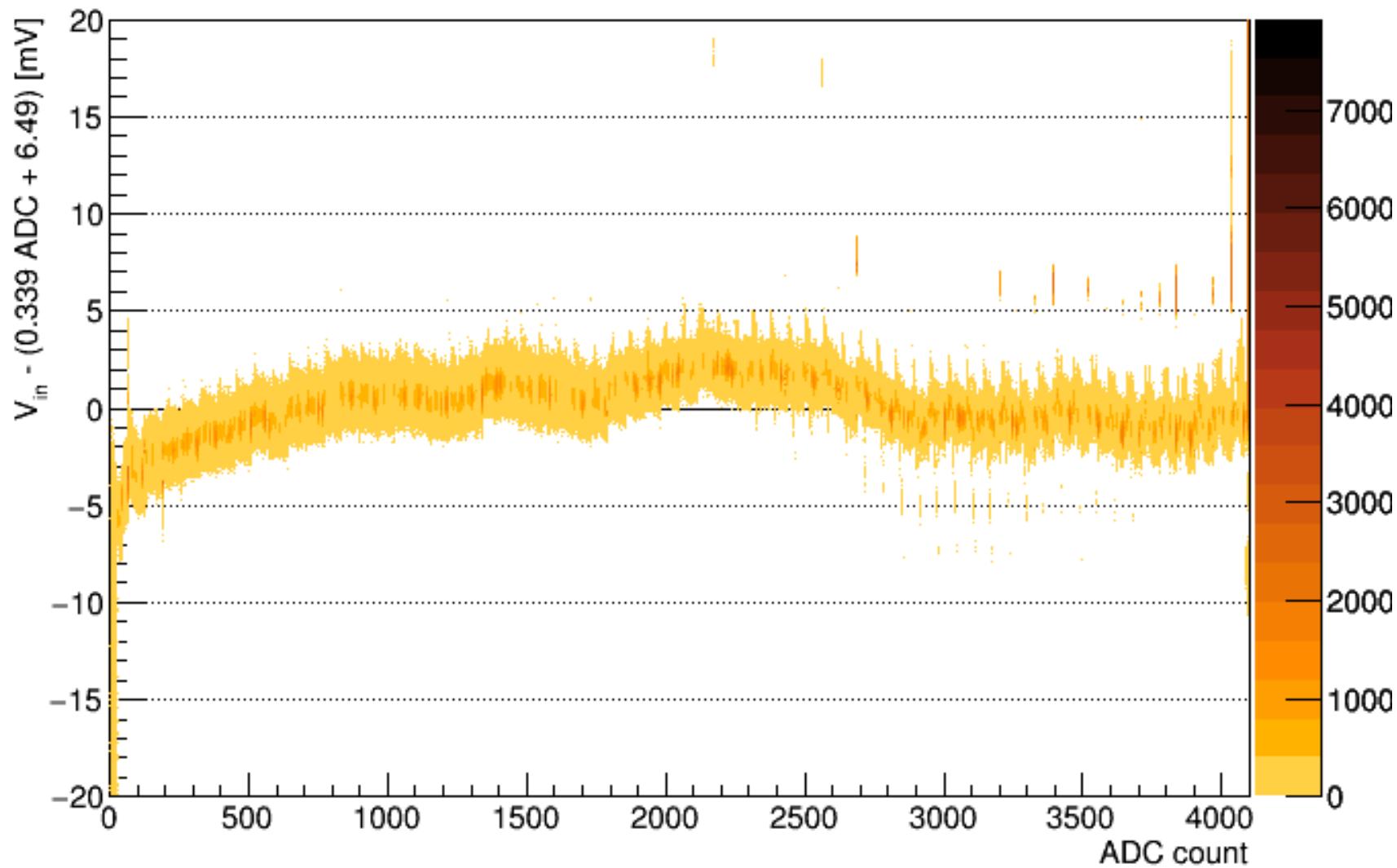
Chip D02, time 1a

201703b_D02_1a channel 6



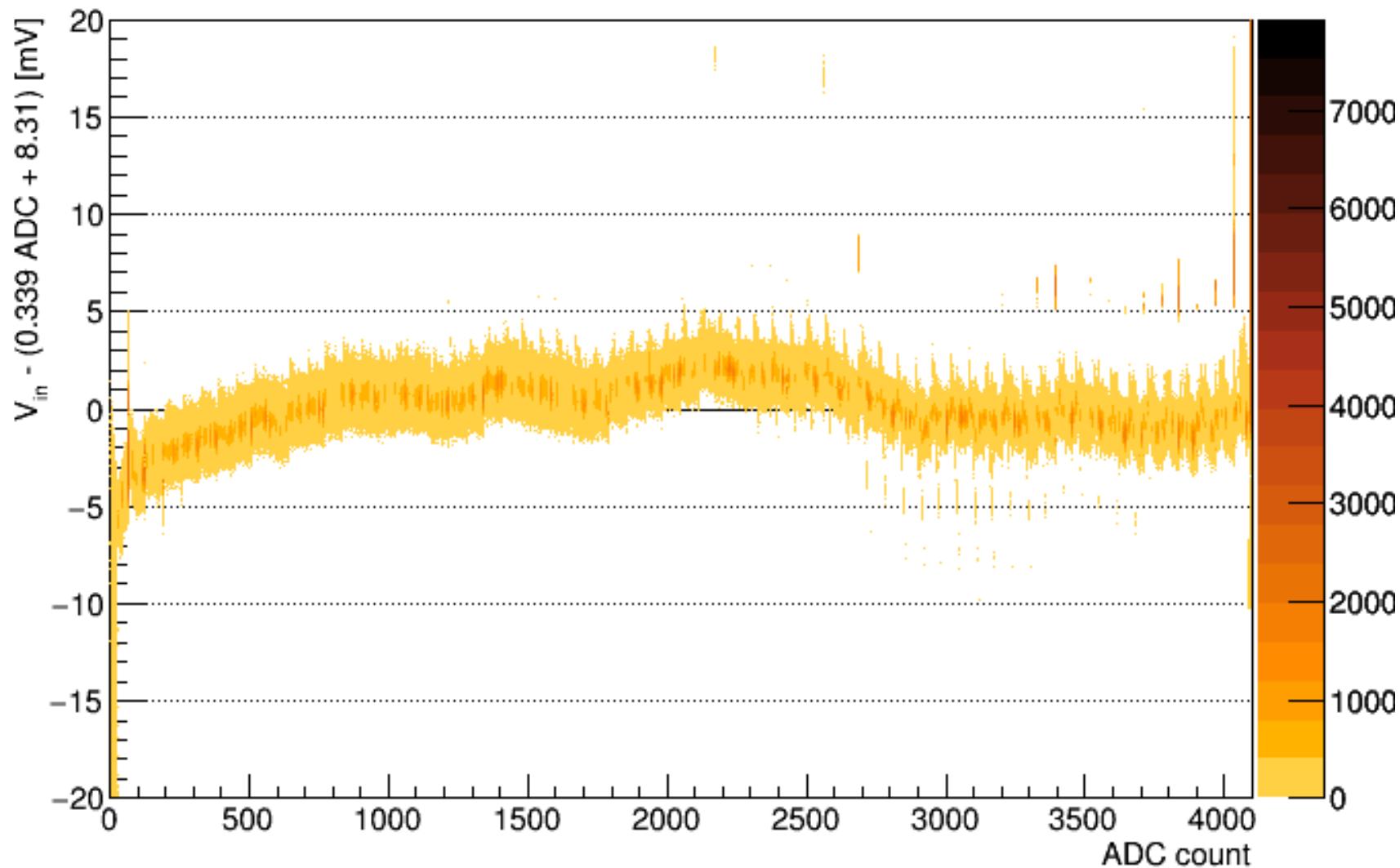
Chip D02, time 2a

201703b_D02_2a channel 6



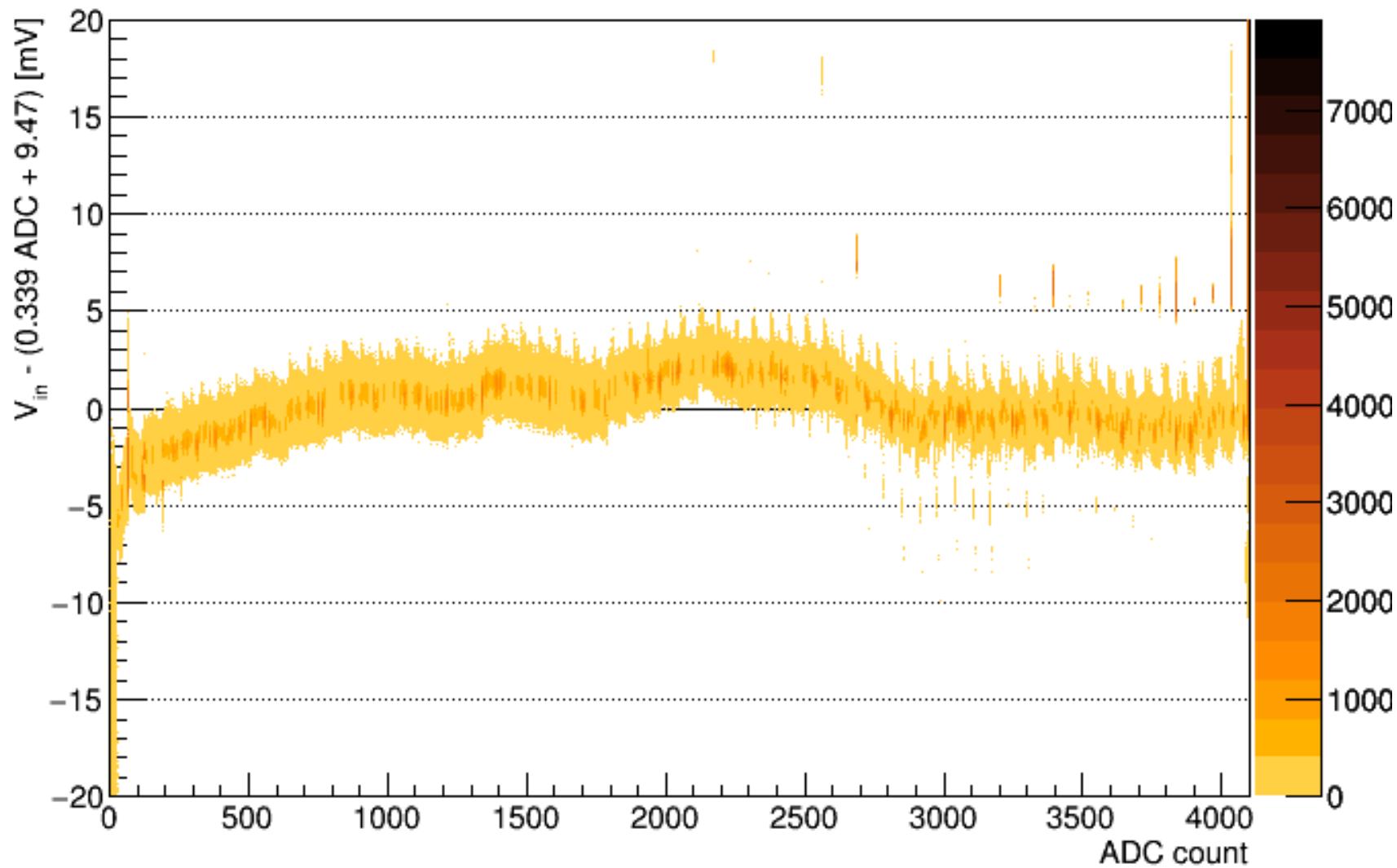
Chip D02, time 3a

201703b_D02_3a channel 6



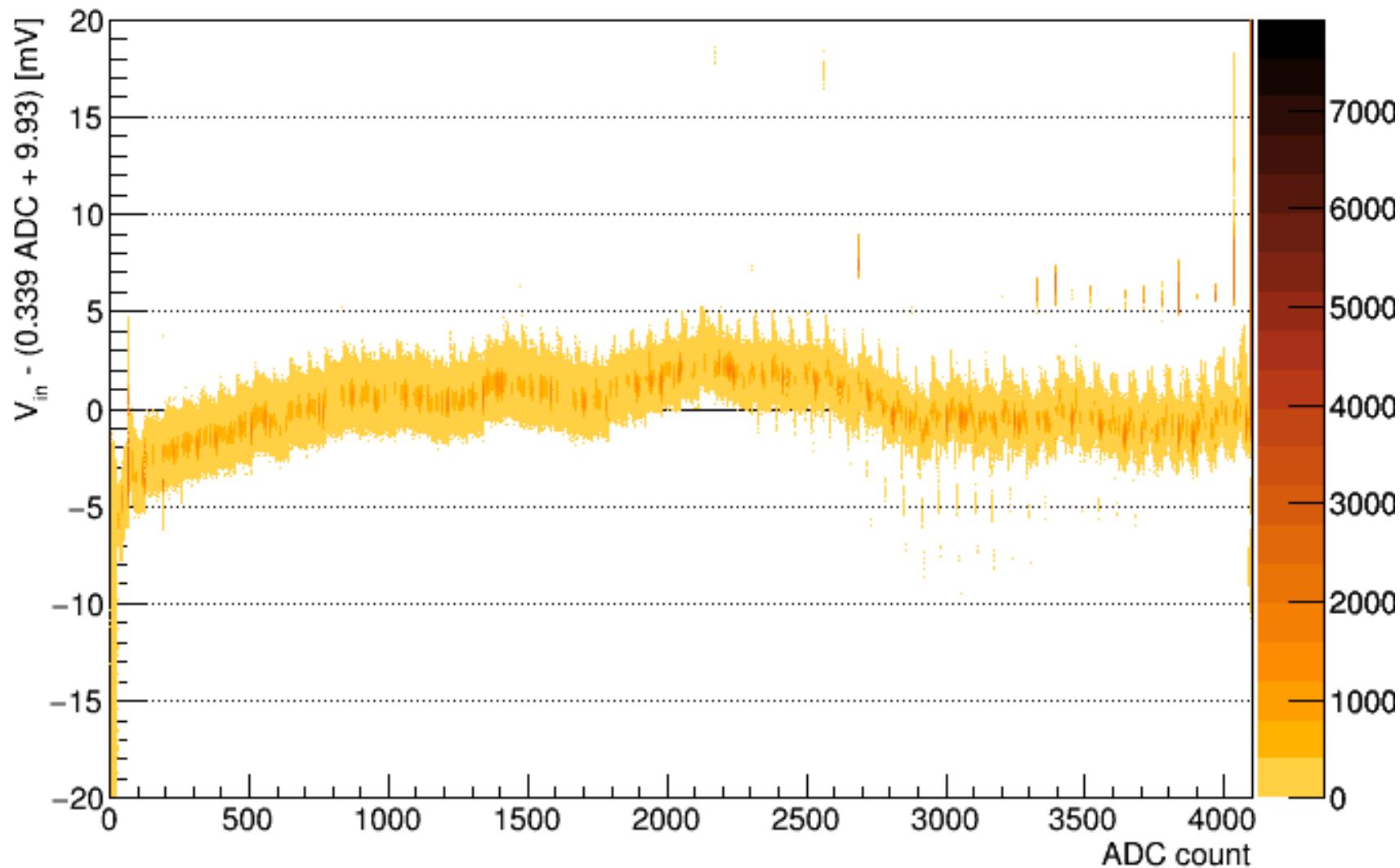
Chip D02, time 3b

201703b_D02_3b channel 6



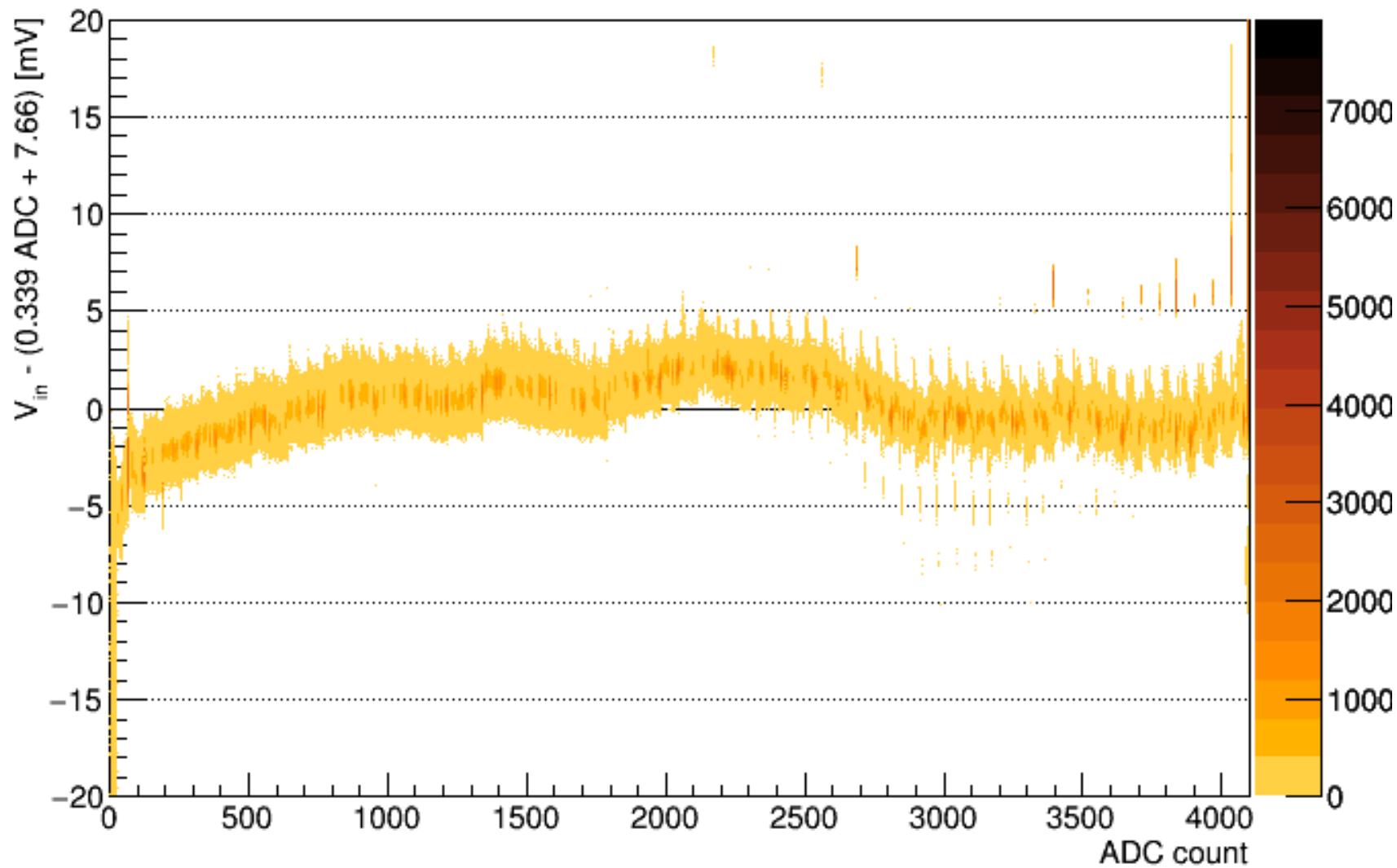
Chip D02, time 4a

201703b_D02_4a channel 6



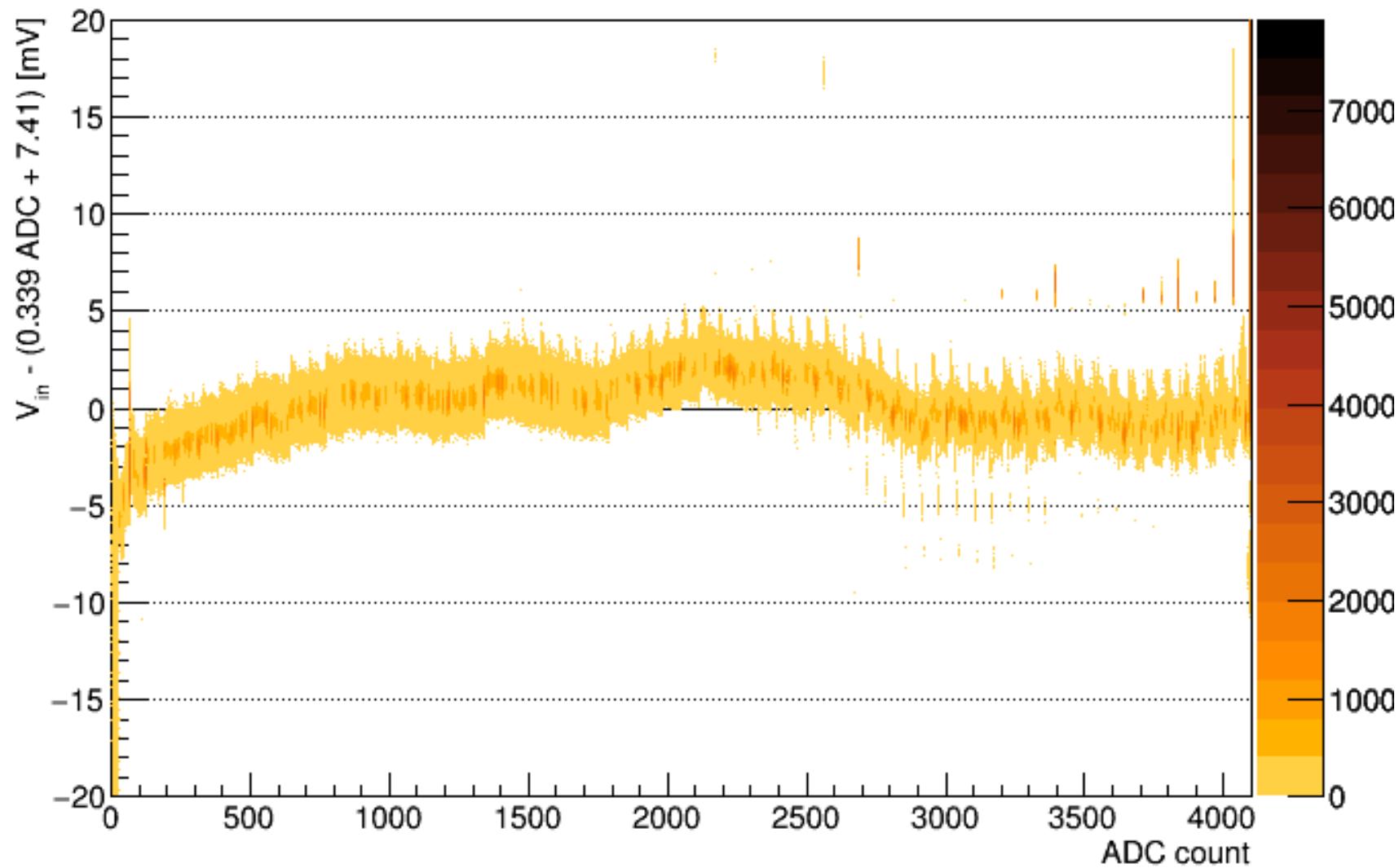
Chip D02, time 4b

201703b_D02_4b channel 6



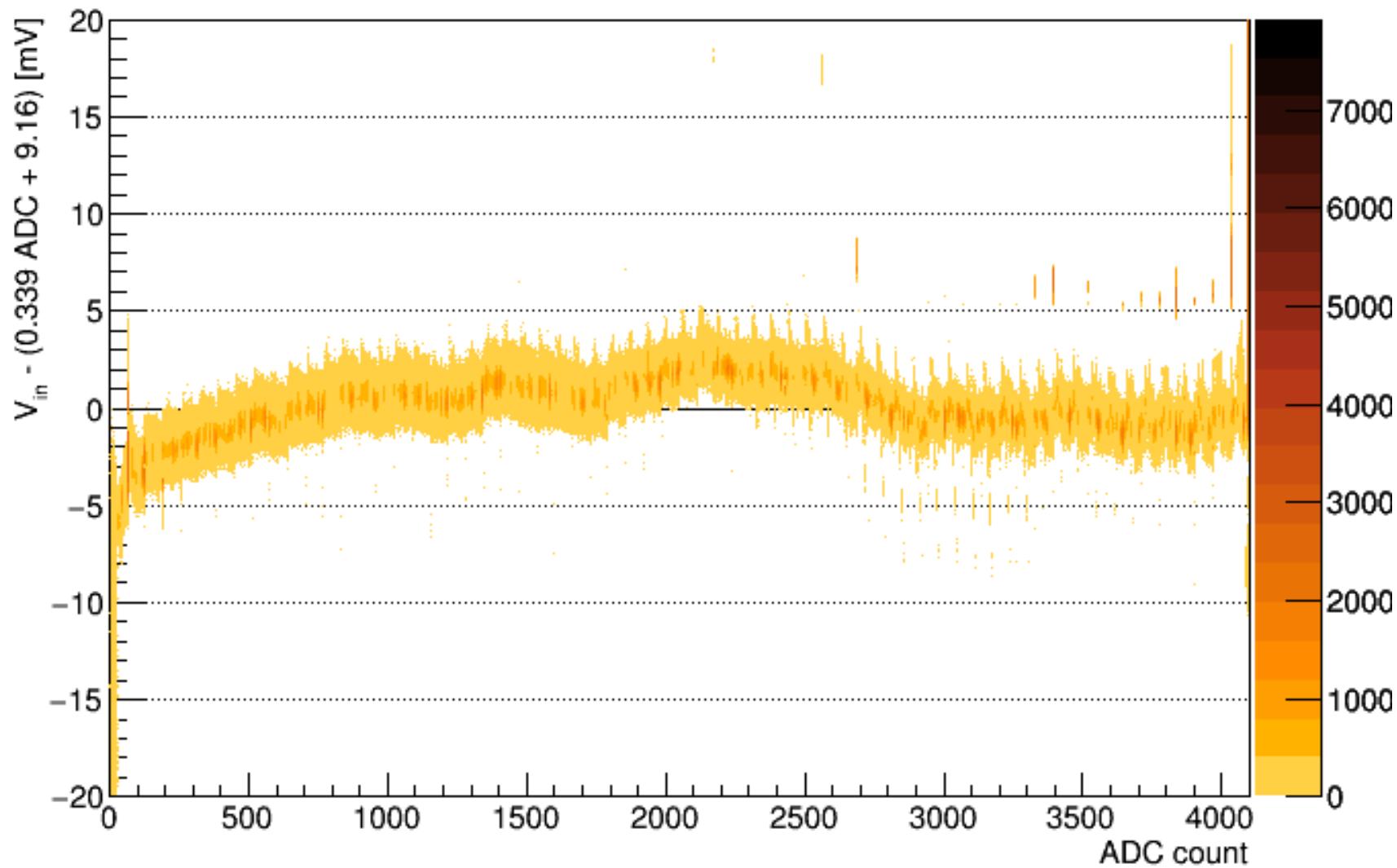
Chip D02, time 5a

201703b_D02_5a channel 6



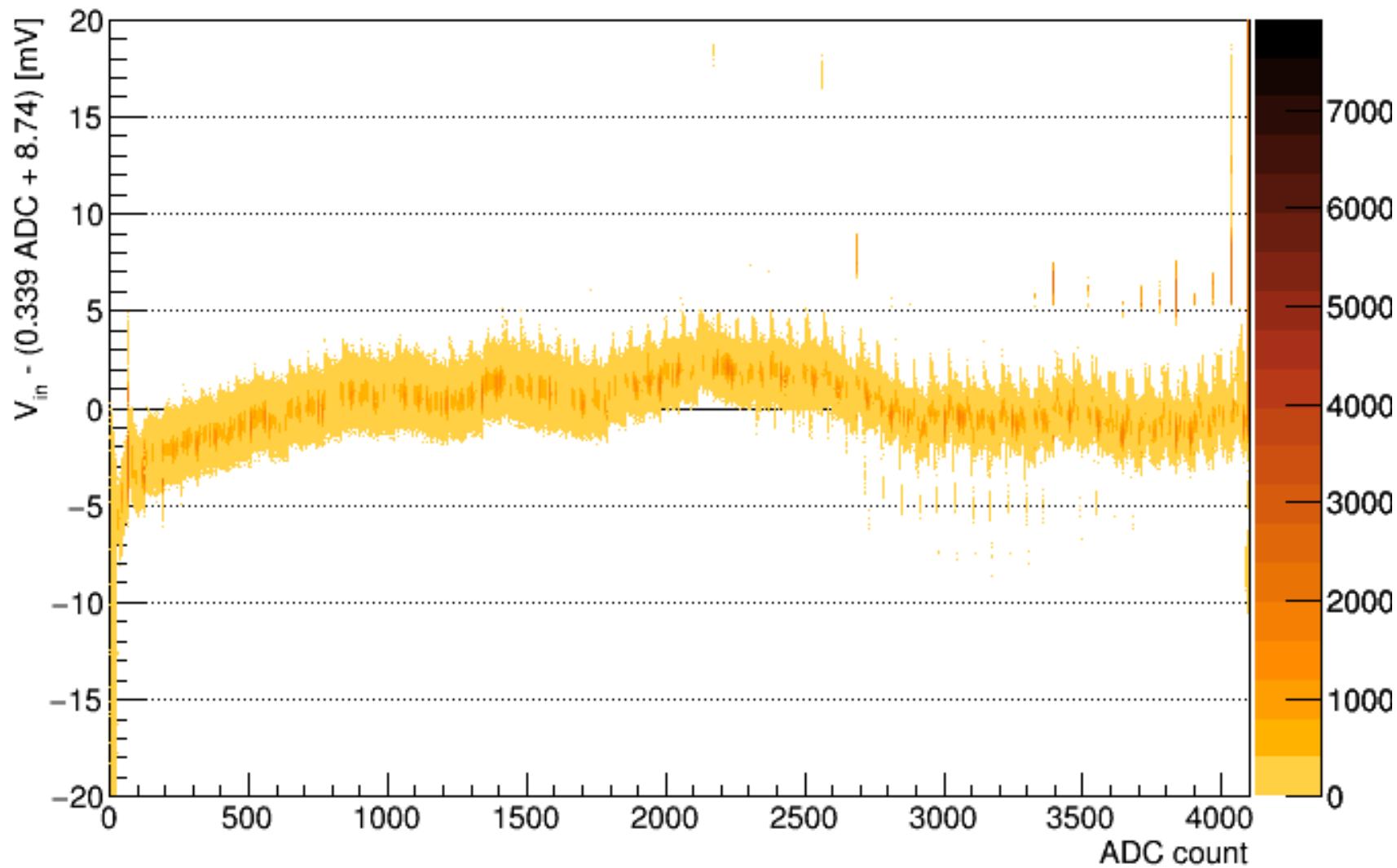
Chip D02, time 5b

201703b_D02_5b channel 6



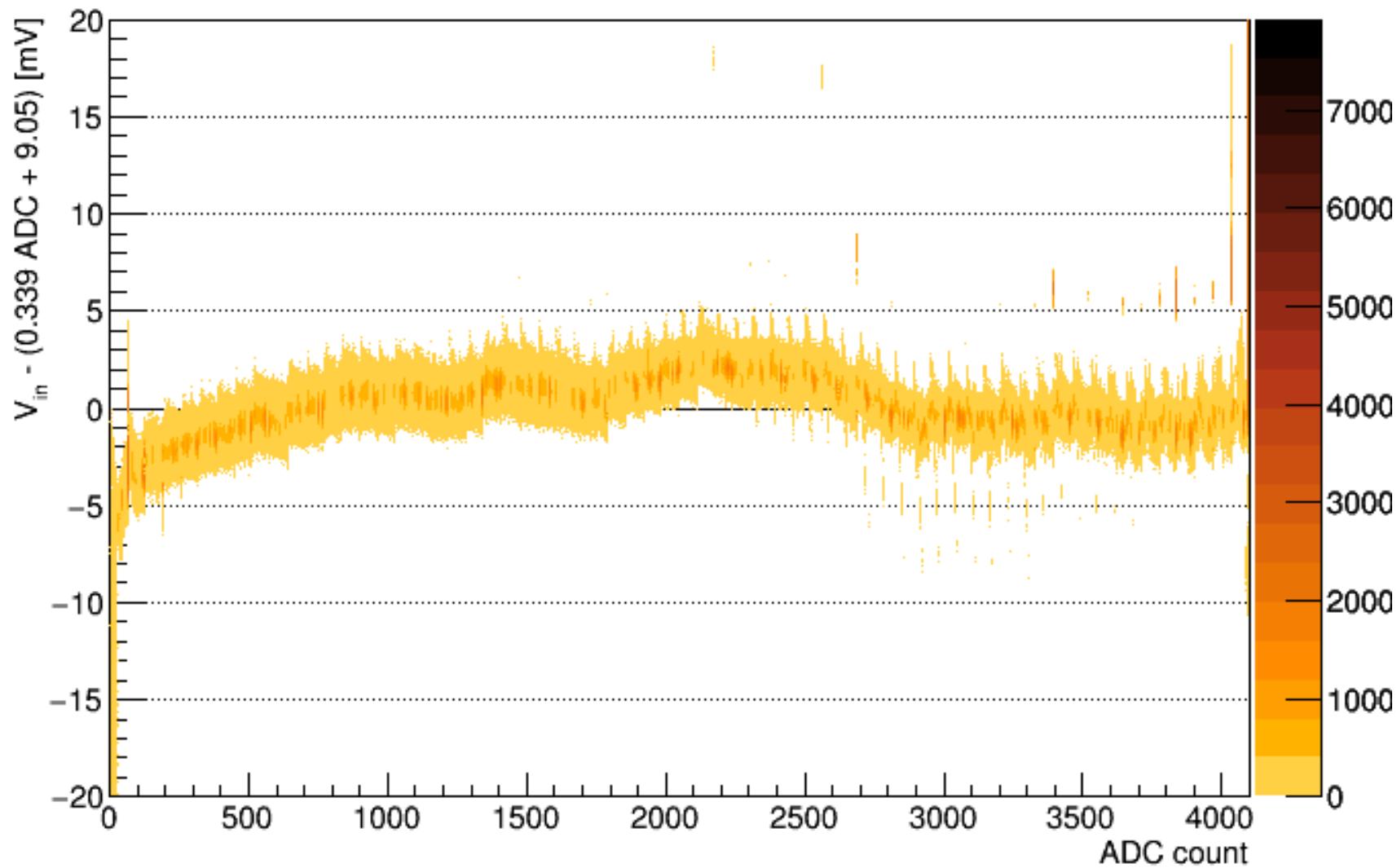
Chip D02, time 6a

201703b_D02_6a channel 6



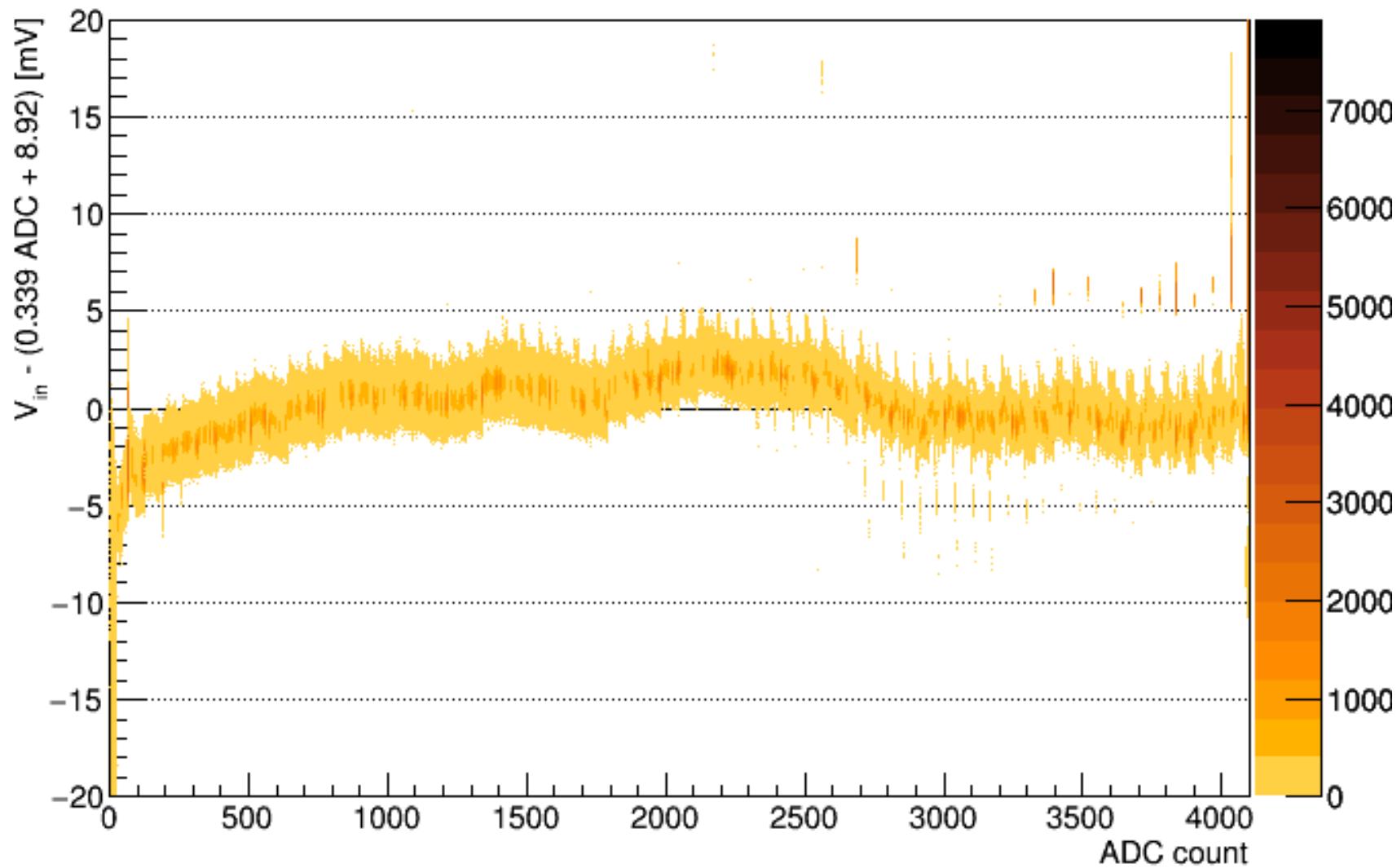
Chip D02, time 6b

201703b_D02_6b channel 6



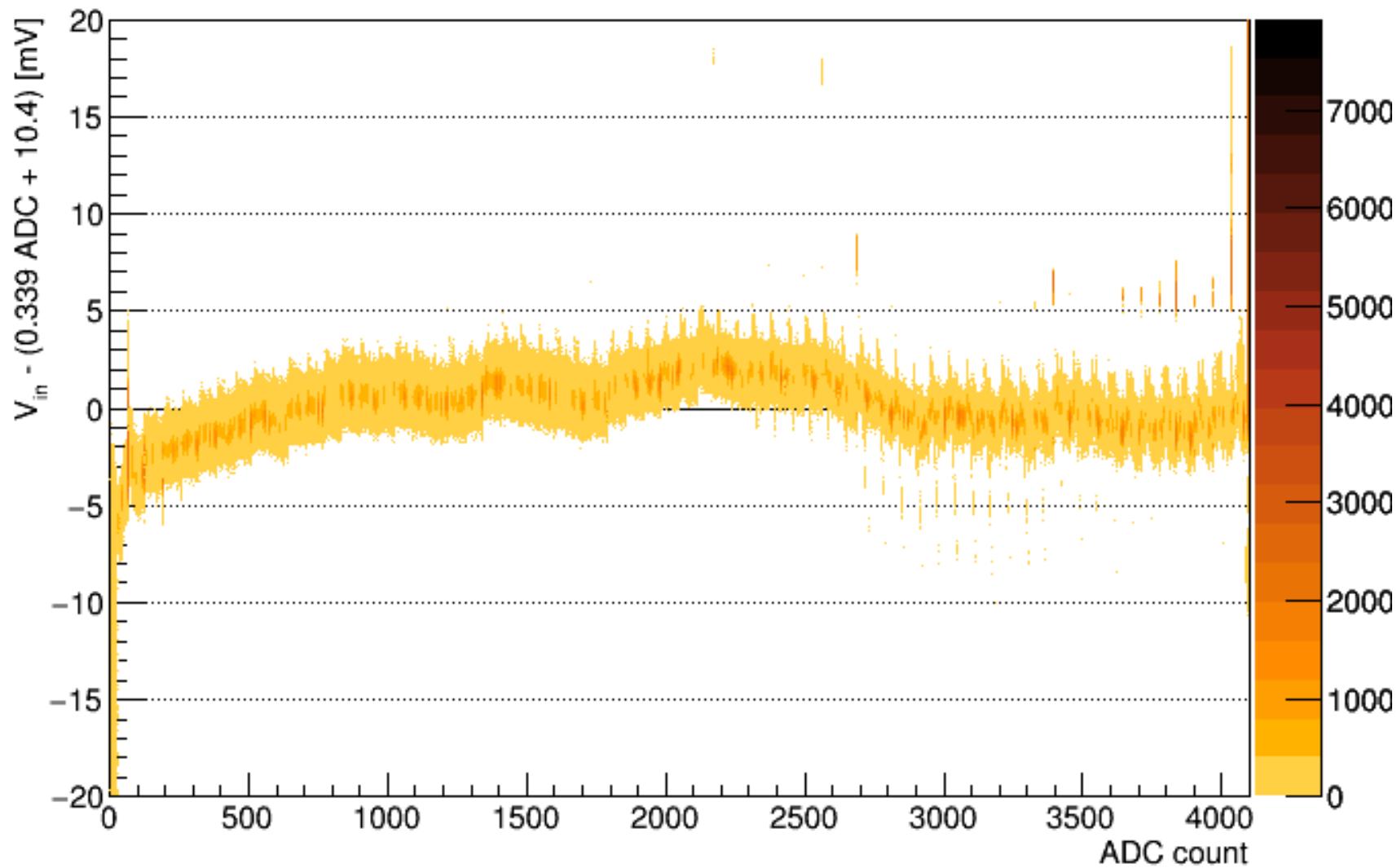
Chip D02, time 7a

201703b_D02_7a channel 6



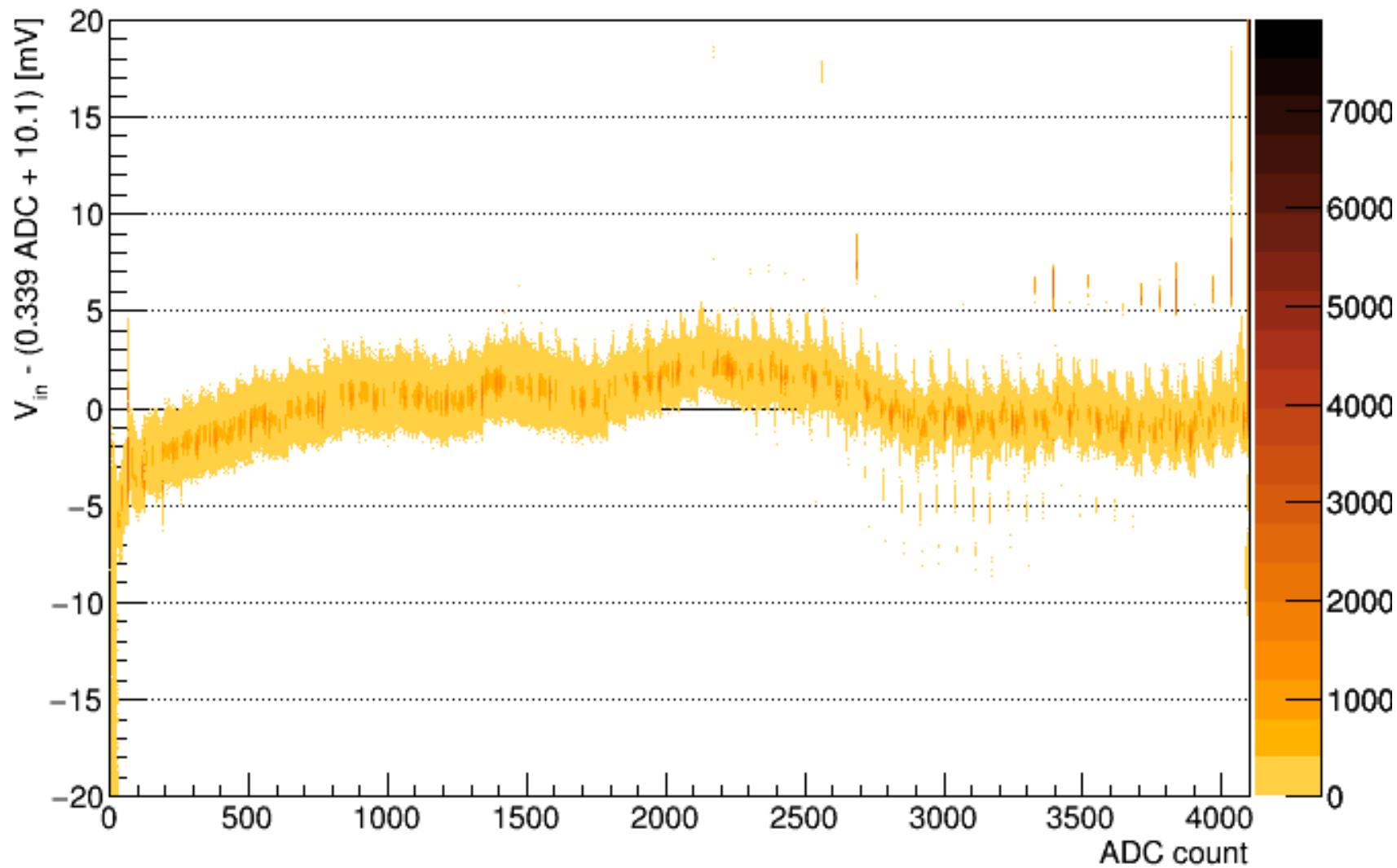
Chip D02, time 7b

201703b_D02_7b channel 6



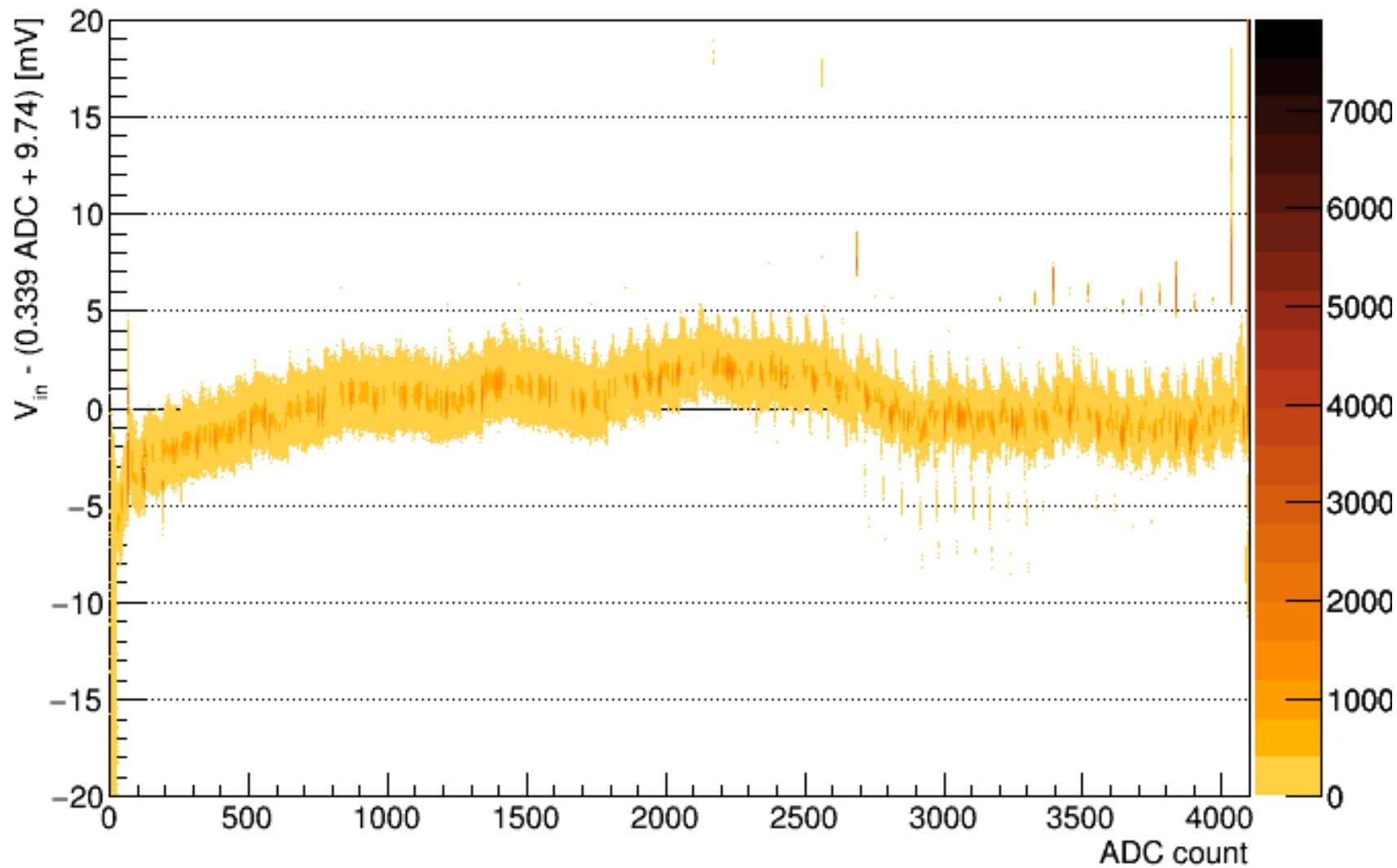
Chip D02, time 8a

201703b_D02_8a channel 6



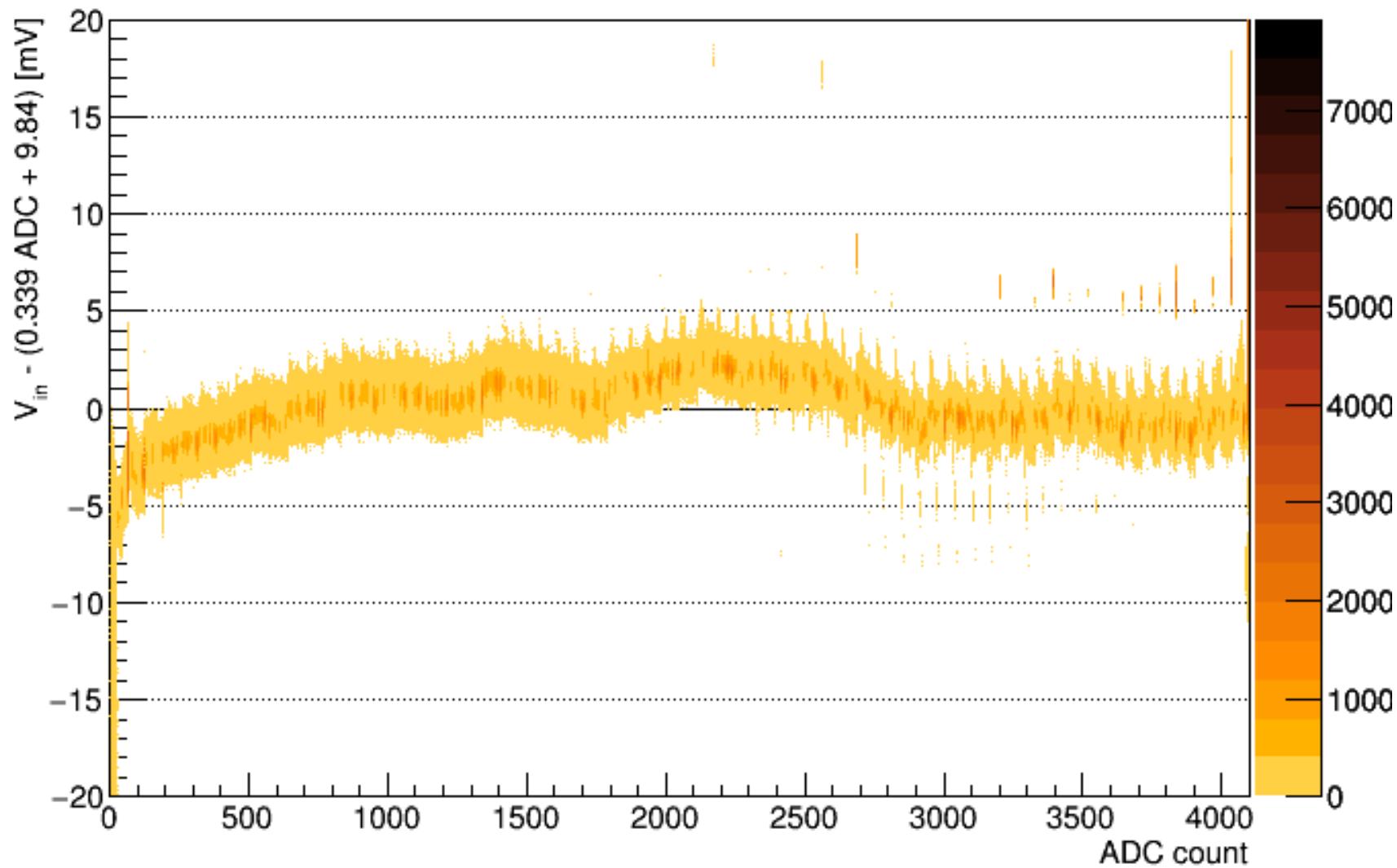
Chip D02, time 8b

201703b_D02_8b channel 6



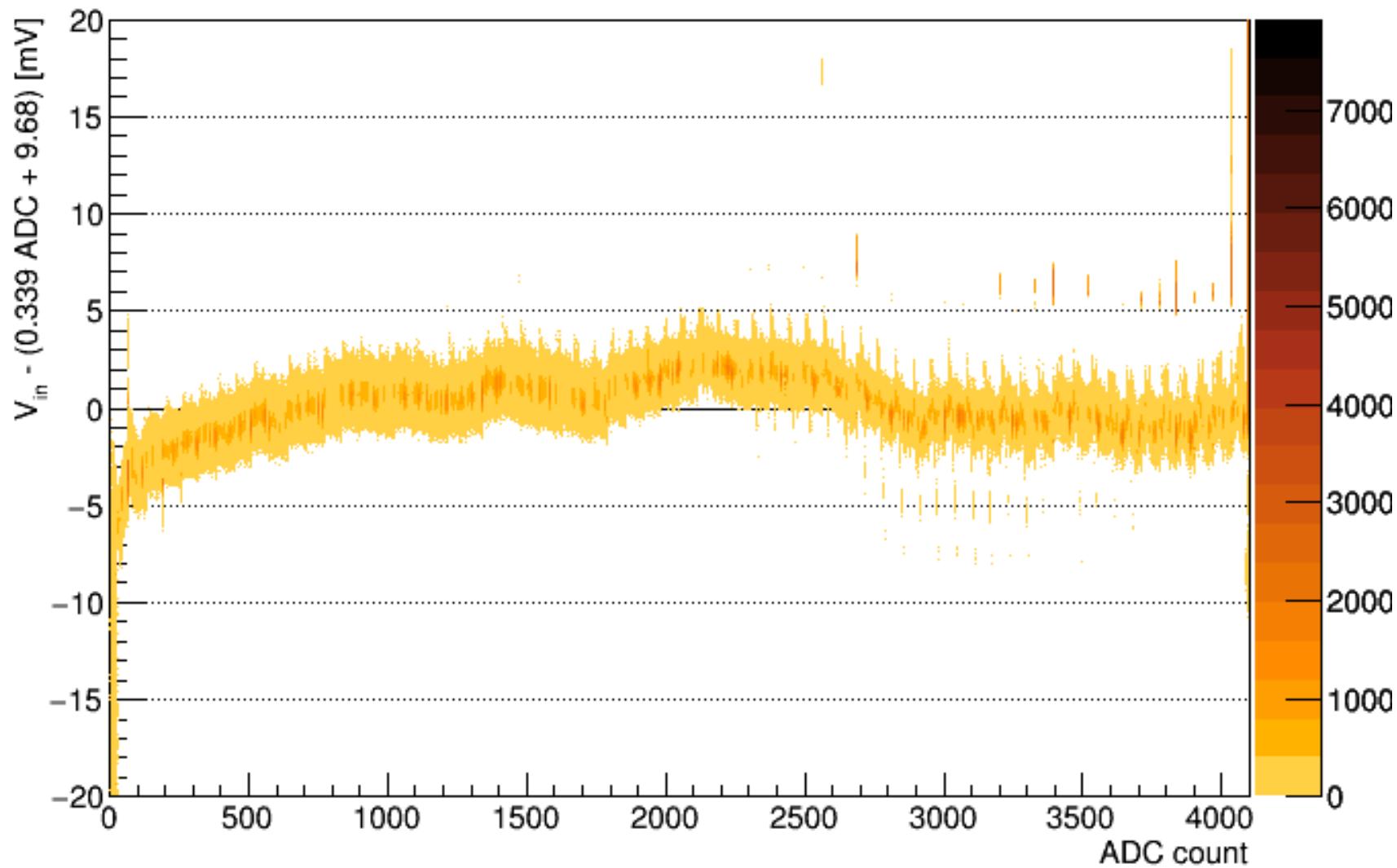
Chip D02, time 8c

201703b_D02_8c channel 6



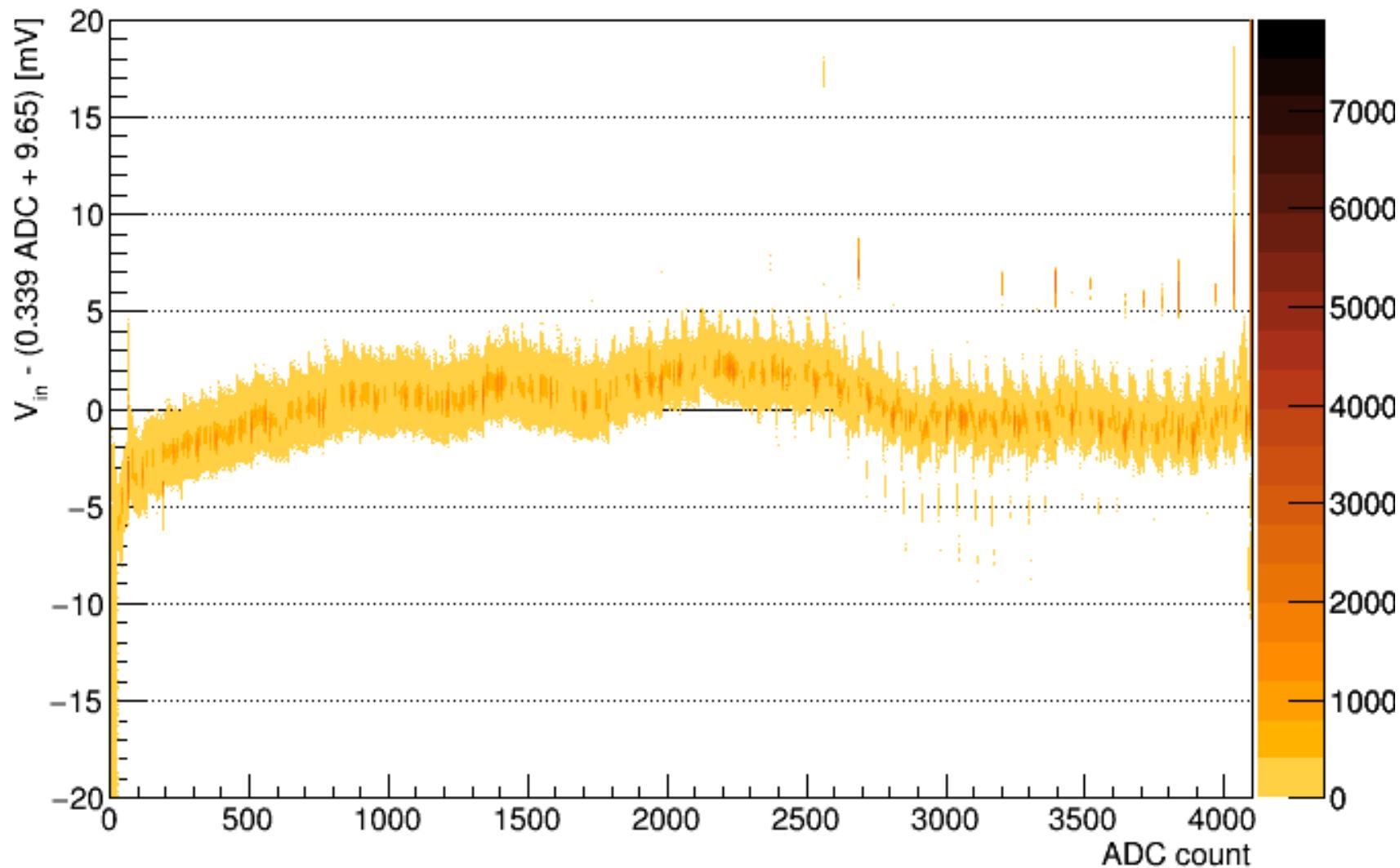
Chip D02, time 9a

201703b_D02_9a channel 6



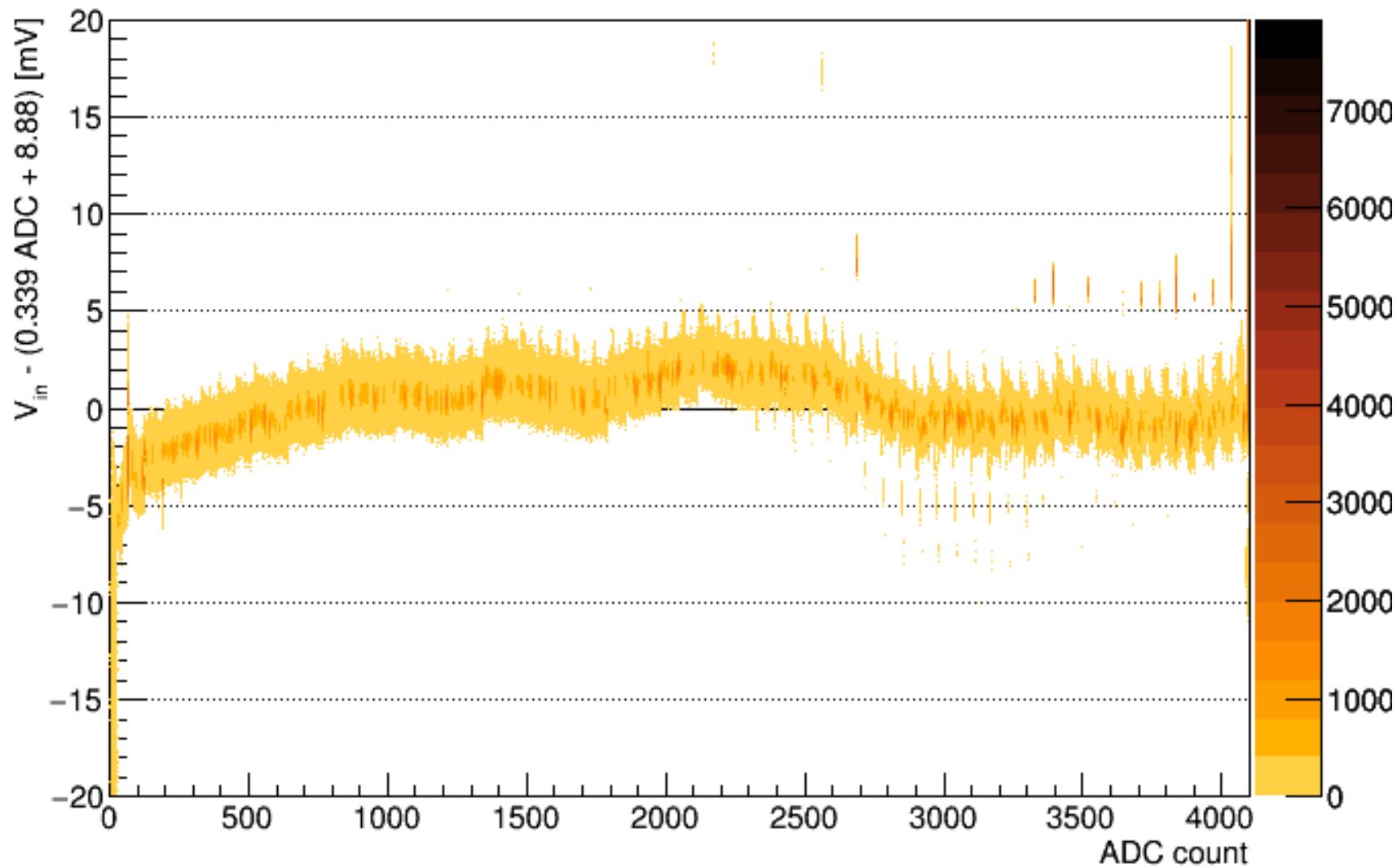
Chip D02, time 9b

201703b_D02_9b channel 6



Chip D02, time 9c

201703b_D02_9c channel 6



How significant is time dependence?

I looked for channels which are sometimes bad

- I.e. RMS < 1.0 for some times and > 1.0 for others
- Table give % bins always good, always bad and varying for each channel

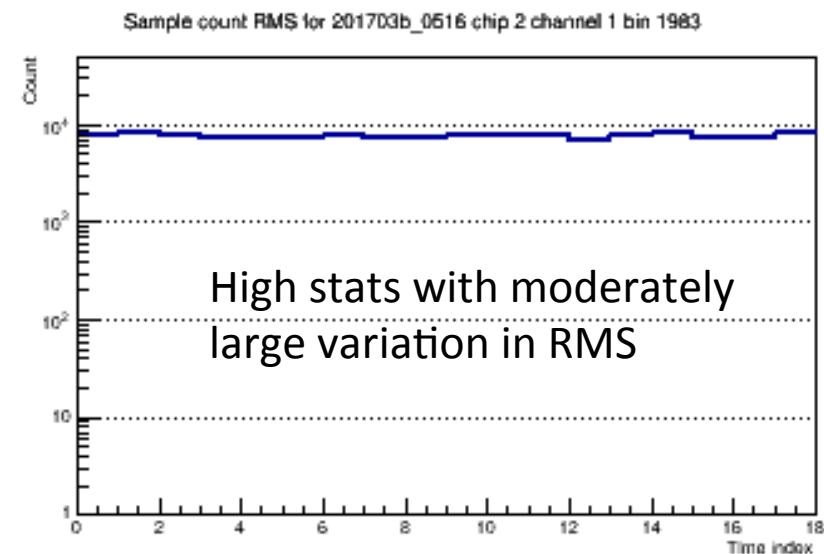
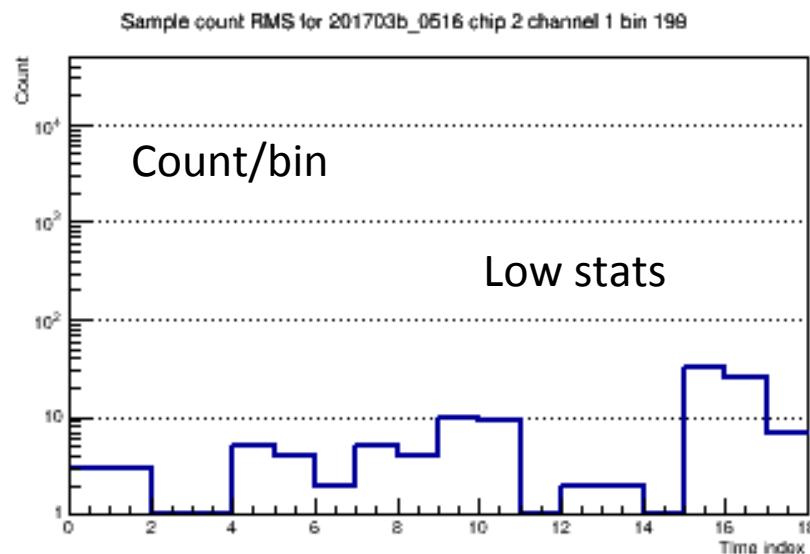
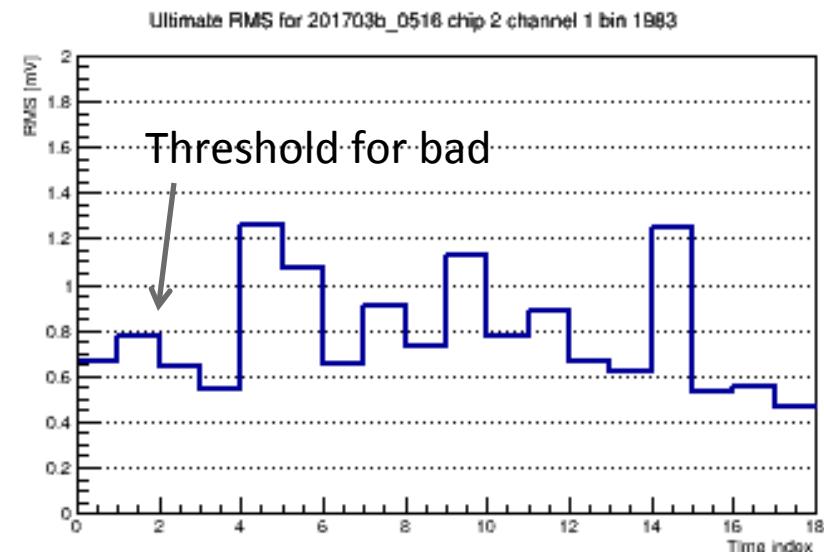
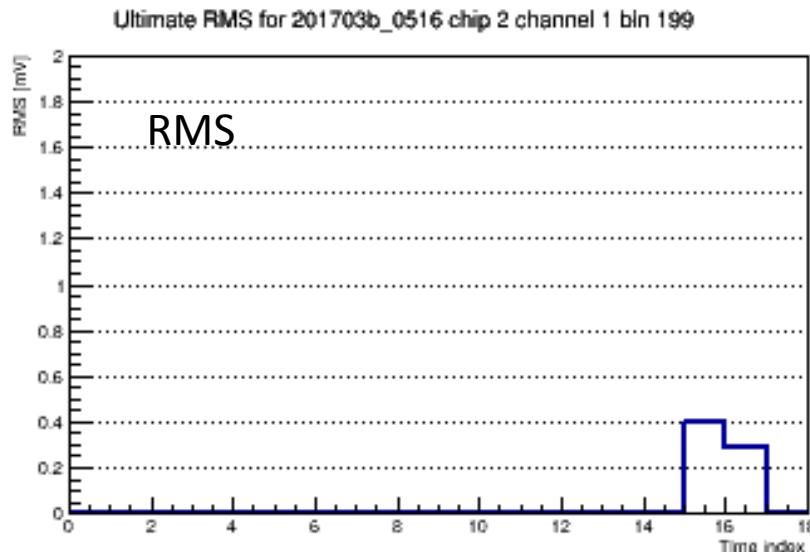
Chan	good	bad	vary	Chan	good	bad	vary
0	88.4	4.6	7.0	8	99.5	0.2	0.3
1	96.5	3.1	0.4	9	94.3	3.1	2.5
2	97.2	1.7	1.1	10	98.1	1.5	0.3
3	97.4	2.0	0.6	11	98.6	0.9	0.4
4	94.5	4.5	0.9	12	94.5	4.2	1.2
5	97.4	2.0	0.6	13	98.4	1.2	0.4
6	97.1	2.1	0.8	14	99.6	0.2	0.2
7	99.0	0.5	0.4	15	98.7	1.0	0.2

Significance of time variation (cont.)

Significant fraction of bins show variation

- But these may have low sample population
- Or may be right on the threshold
- See plots in appendix 3
 - One example on following page
- More work needed to quantify behavior

Time varying bins 6



Comments/Conclusions

ADC does show some time dependence

- For chip in board, kept cold and powered
- Gain is very stable
- Residual from linear calibration is also pretty stable
- But there are changes in bad channels (RMS) and tails day-to-day
 - Probably want to look at multiple ramps to identify all bad/tail channels

Next

- Quantify changes in bad channels and tails

Appendix 1

Analysis procedure is described on the following slides

Data analysis 1: linear fit and residual

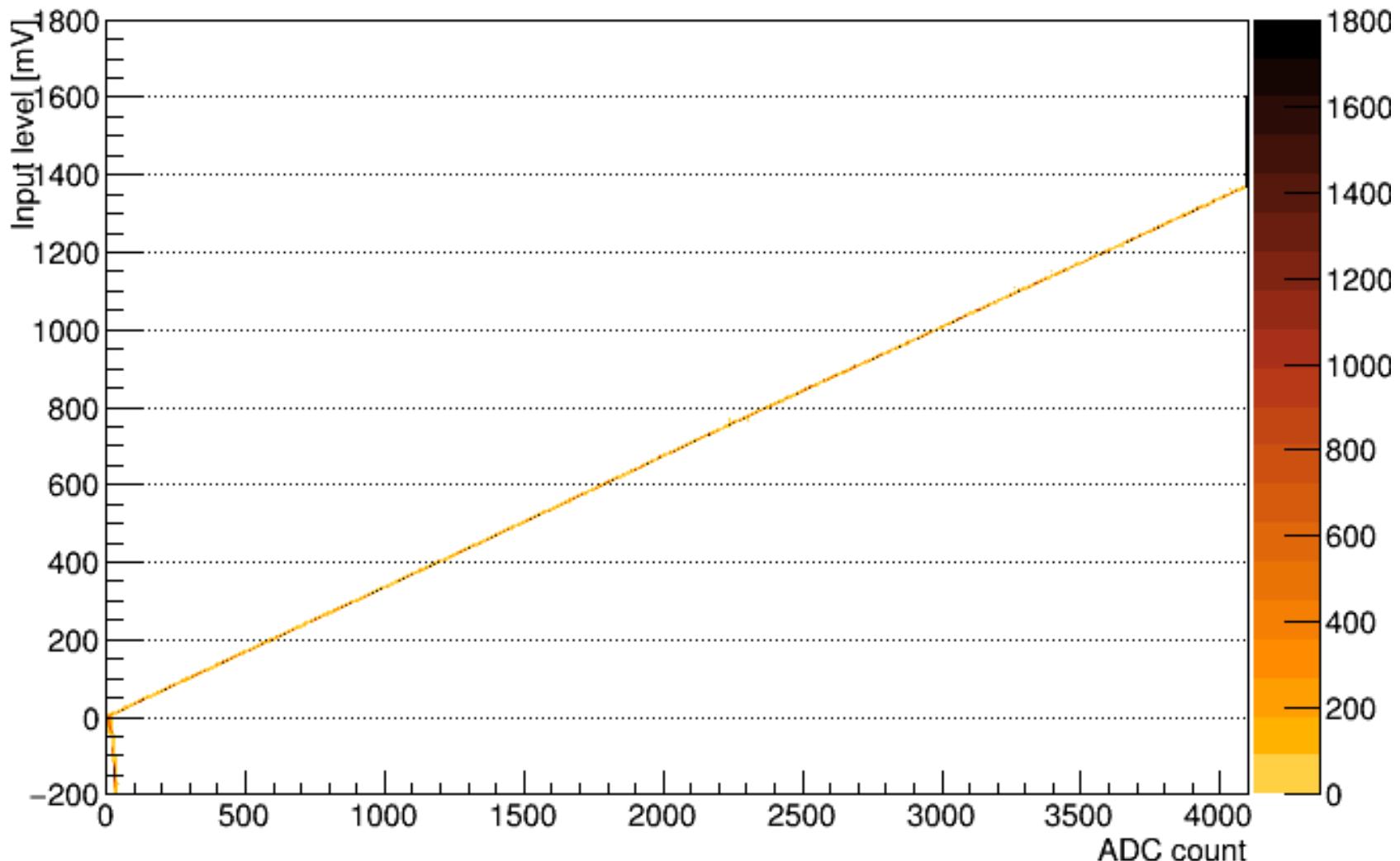
I process each channel separately

Initial data analysis

- Read samples from the provided file for the chip and channel
- Create 2D histograms of inverse response: V_{in} vs. bin
 - bin = ADC code and covers the range [0, 4095]
- I make a linear fit of the inverse response for each channel
 - $V_{in} = \text{gain} \times (\text{ADC code}) + \text{offset}$
 - Require $64 < \text{ADC} < 4095$
 - And $0 < V_{in} < 1600 \text{ mV}$
- I then plot the linear-fit residual
 - I.e. the difference between the measured V_{in} and the linear-fit value for each sample
- Examples for one channel follow
 - March data for chip D04 channel 7
 - This is a “good” channel

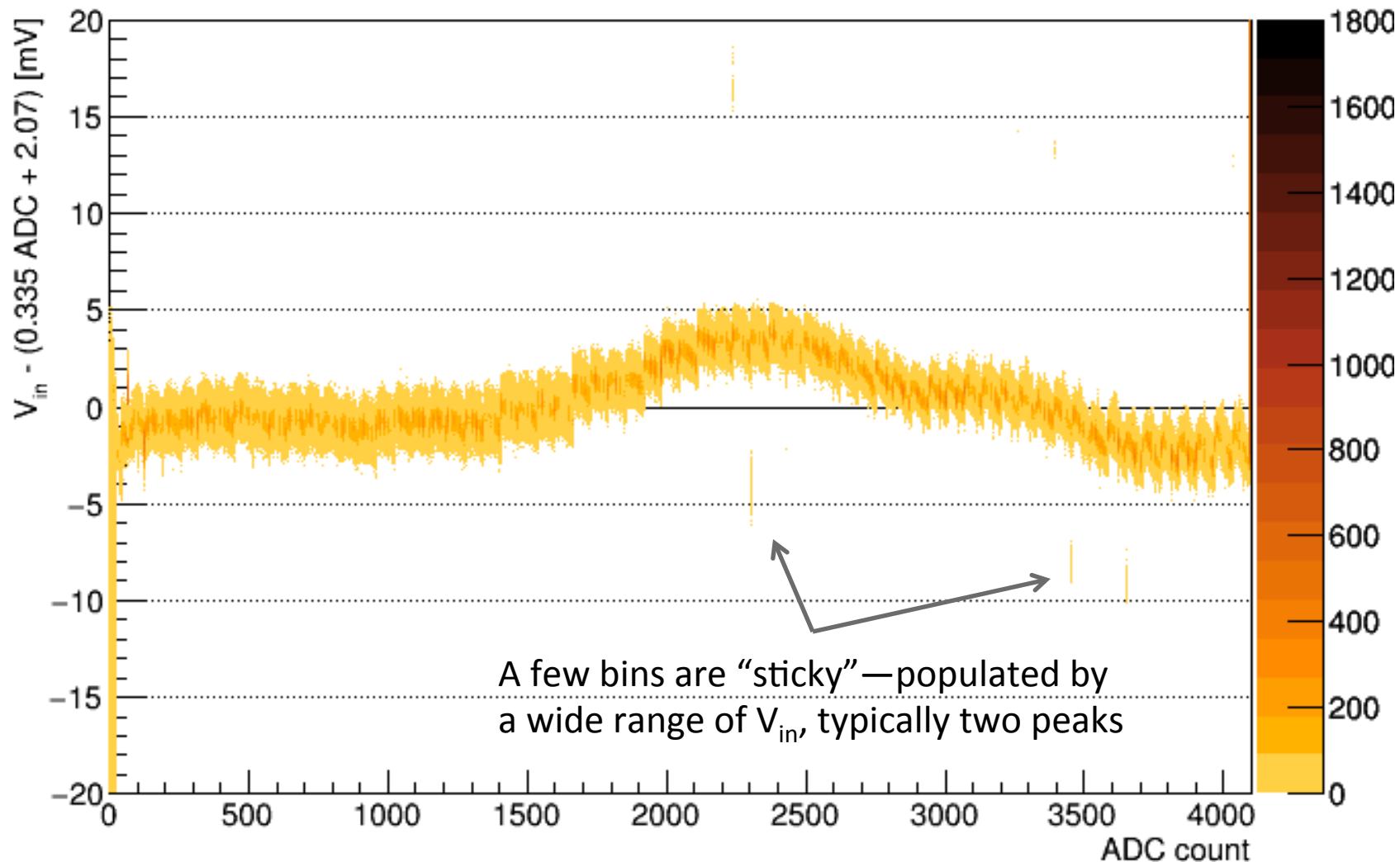
Inverse response

201703a_D04 channel 7



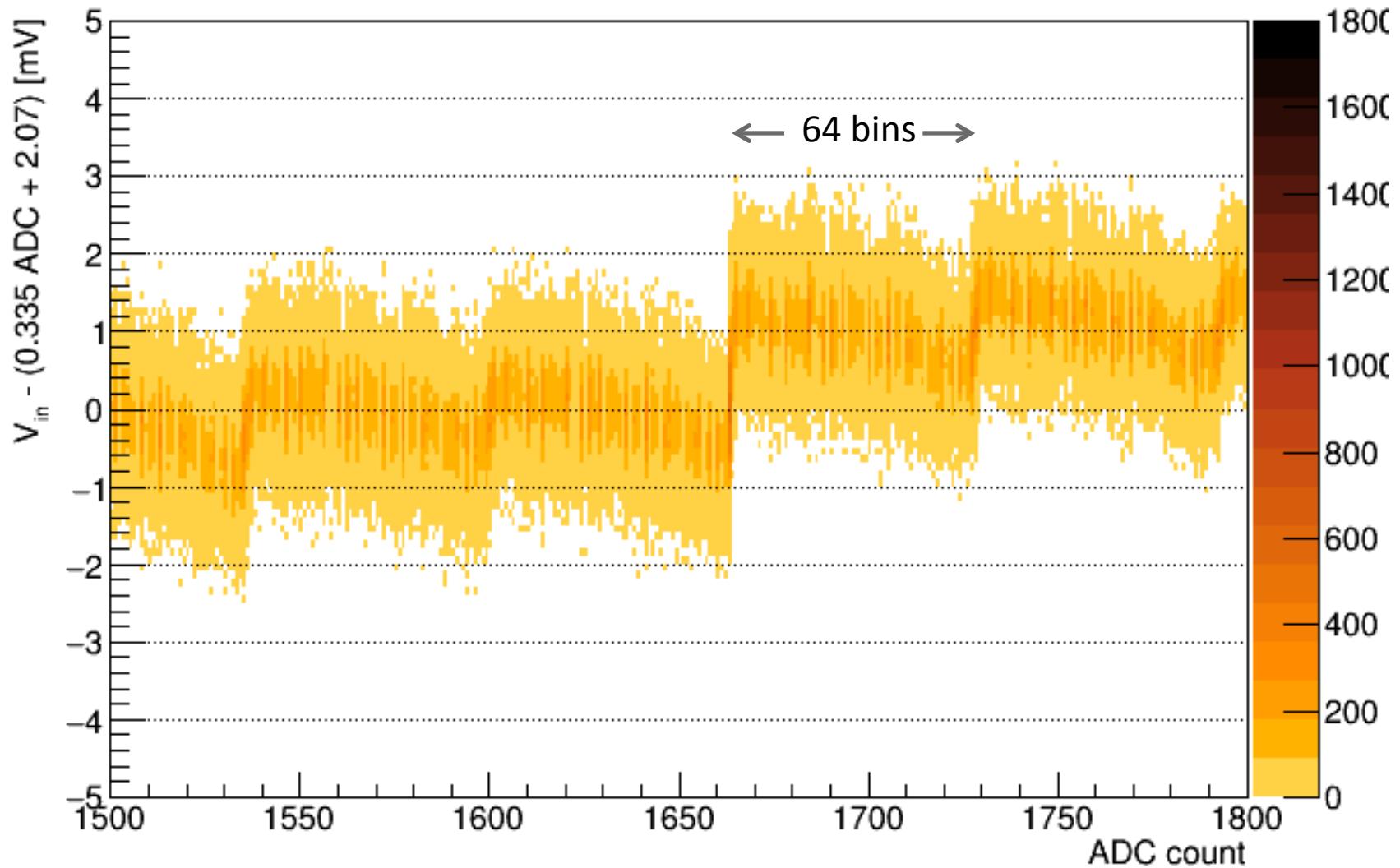
Linear fit residual

201703a_D04 channel 7



Linear fit residual zoomed

201703a_D04 channel 7



Data analysis 2: calibration and resolution

From fit and residual, define ultimate calibration for each bin

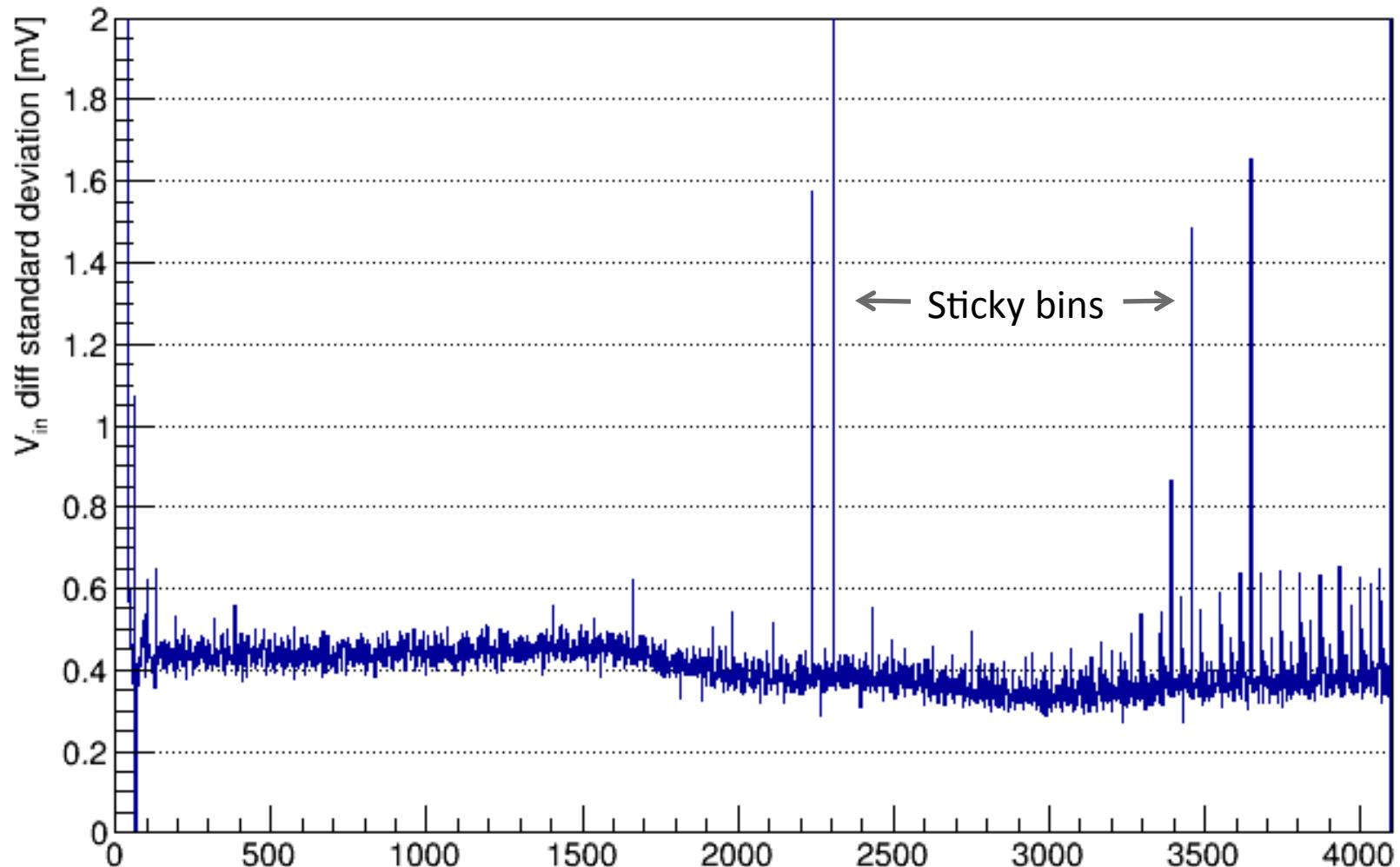
- Mean of the residual plus the linear fit is the calibrated value
- I.e. a lookup table for each channel with approximately 4000 entries
- May not be final calibration strategy but this is the best we can do

Ultimate resolution

- The spread in V_{in} provides a measure of the uncertainty in the voltage measurement for each bin
- Characterize this with the standard deviation, the RMS from the mean
- Typical example follows (again a “good” channel)
- Typically this is around 0.5 mV
 - Naïve expectation for perfect 12-bit ADC is 0.1 mV
- Following page shows the distribution for all chips

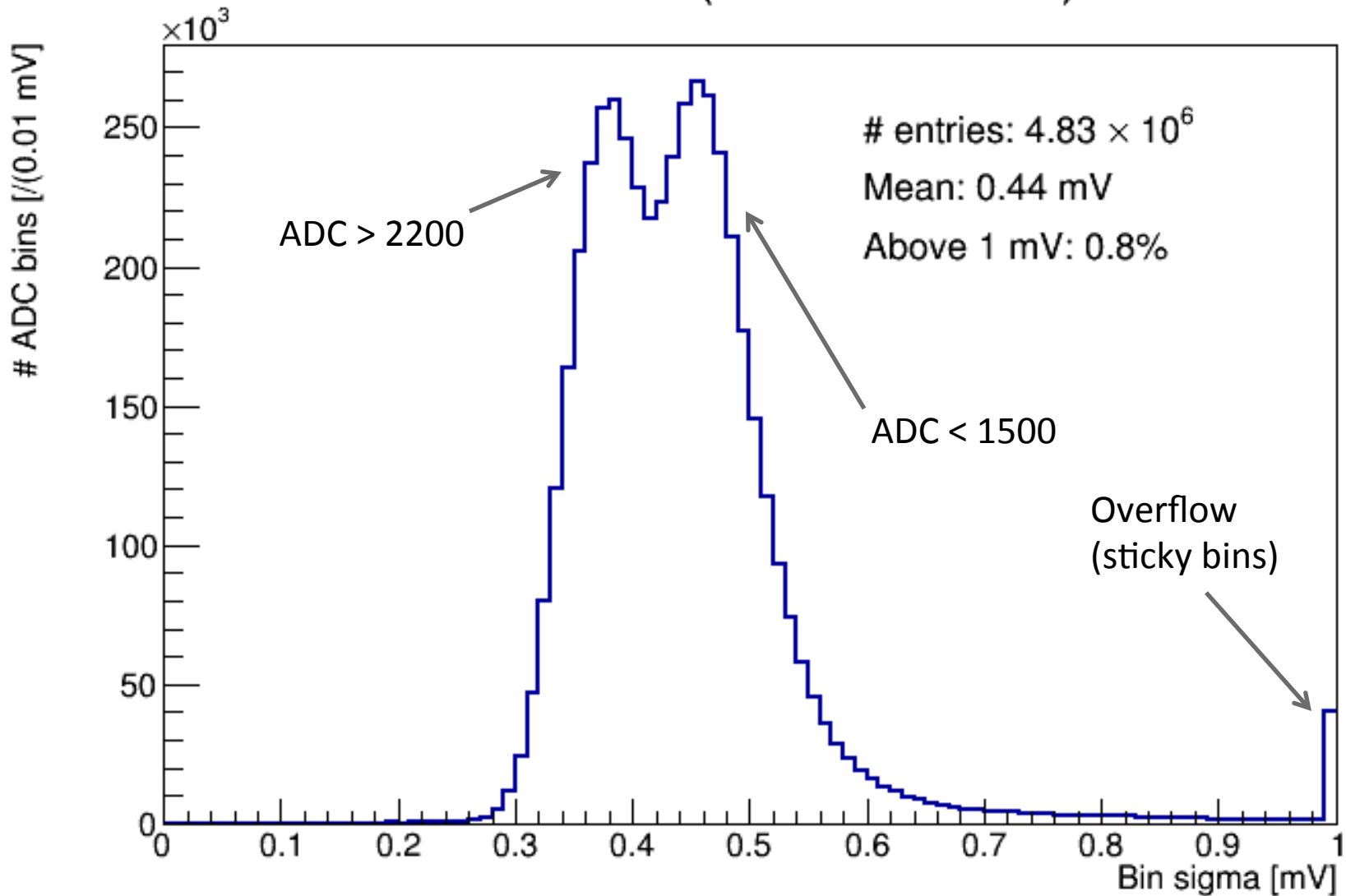
Ultimate resolution for one channel

201703a_D04 channel 7 fit sigma



Ultimate resolution for all chips

ADC bin resolution ($65 < \text{ADC} < 4095$)



Data analysis 3: sticky bins

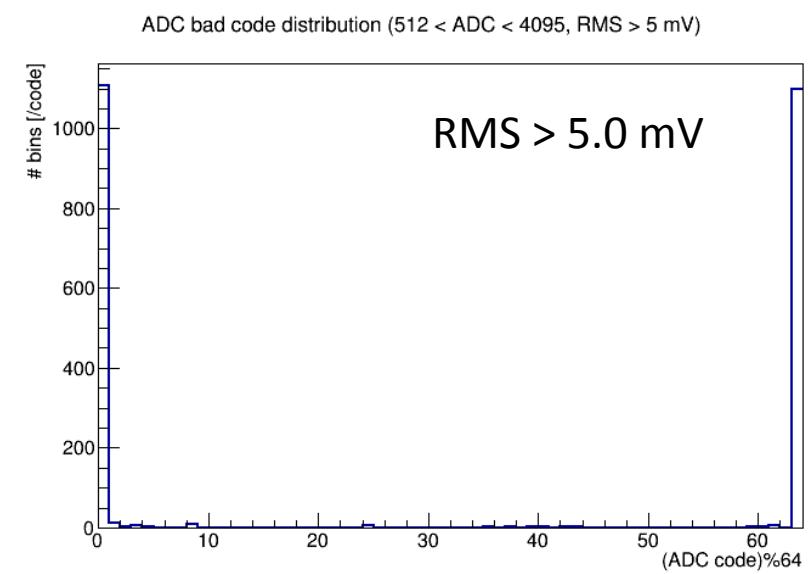
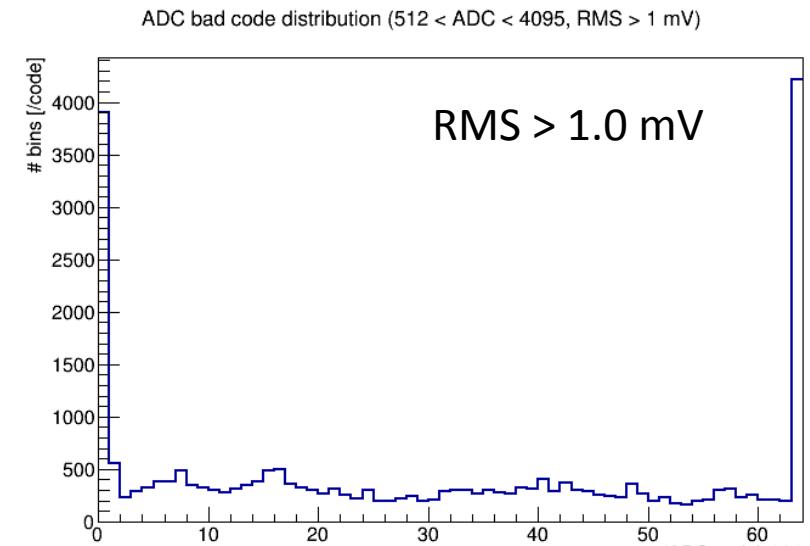
Sticky bins

- There are always a few (sometimes many) bins populated by a wide range of input voltage
 - Can be identified by poor resolution i.e. large RMS
 - Often bins where LSB6 (lower six bits) are all 0 or all 1
 - Often a double peak where one peak is in the expected place
- Distribution for March 2017 data shown on following slide
 - 25 chips → 400 channels → 1.6M bins
- When resolution for a bin is too large, we can get better precision by discarding that measurement and interpolating between neighboring bins
- Plan to maintain a list of sticky bins for each channel so we know which bins to discard
 - Use the resolution (RMS from mean) to identify sticky bins
 - Here define sticky as $\text{RMS} > 1.0 \text{ mV}$
 - This is equivalent to an input noise of 450 e for preamp gain 14 mV/fC

Sticky bins: LSB6 distributions

Plots show LSB6 for bad bins

- LSB6 = six least significant bits
 - I.e. $\text{bin} \% 64$
- For different RMS thresholds
- Classic values of 0 and 63 are enhanced for all thresholds
 - Dominate for high threshold



Data analysis 4: ADC quality

Voltage response

- We evaluate ADC quality as a function of voltage
 - No ADC channel covers the full range of interest (0, 1600) mV
- Evaluate three metrics: efficiency, resolution and tails
- All evaluated as functions of V_{in} in bins of 20 mV
- Results presented in “performance summary plots” (PSPs)
 - Example plot for an ADC bin follows
 - Not the bin used in earlier example plots—instead one with issues

ADC efficiency

- Define efficiency to be fraction of samples that land in good ADC bins
 - For each range of input voltage
 - Good means $RMS(V_{in} \text{ residual}) < 1.0 \text{ mV}$
- Performance summary plots show efficiency vs. V_{in} (blue histogram)
 - Following example is the same “good” channel as in earlier plots
 - Plots for all 76 chips in appendix

Data analysis 4: ADC quality (2)

Resolution

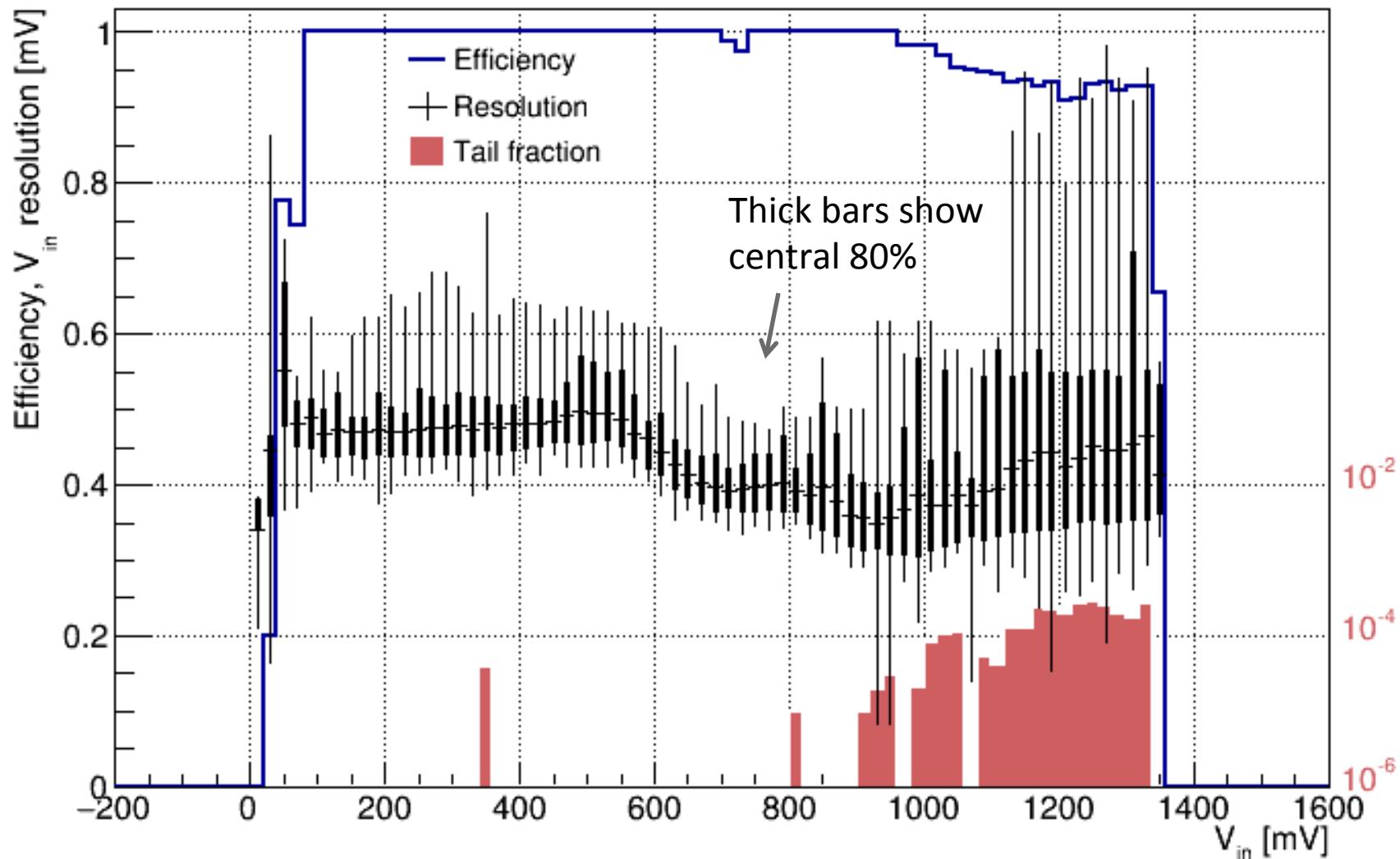
- Resolution vs. V_{in} is shown on the same plot (black markers)
 - Evaluated as the RMS difference between the measured and true V_{in} for each sample in the voltage bin
 - Measured V_{in} is obtained by applying the calibration to the ADC count
 - Horizontal bars indicate the mean of this RMS for each bin
 - Error bars show the extent of the distribution of assigned uncertainties
 - Using all ADC bins populated by the samples in the voltage bin
 - Full range (earlier plots only showed central 80%)
 - Assigned uncertainty for an ADC bin is $\text{RMS}(V_{in} \text{ residual})$

Tail fraction

- The tail fraction is also shown (filled red histogram)
 - Fraction of samples in the voltage bin less than 5 mV from the true V_{in}
 - Previously used 5σ to define tail but this seems too tight
 - Because uncertainty at input to ADC is 1.3 mV
 - » 600 e with a gain of 14 mV/fC

Example performance summary plot

201703a_D20 channel 10 actual performance for RMS < 1 mV



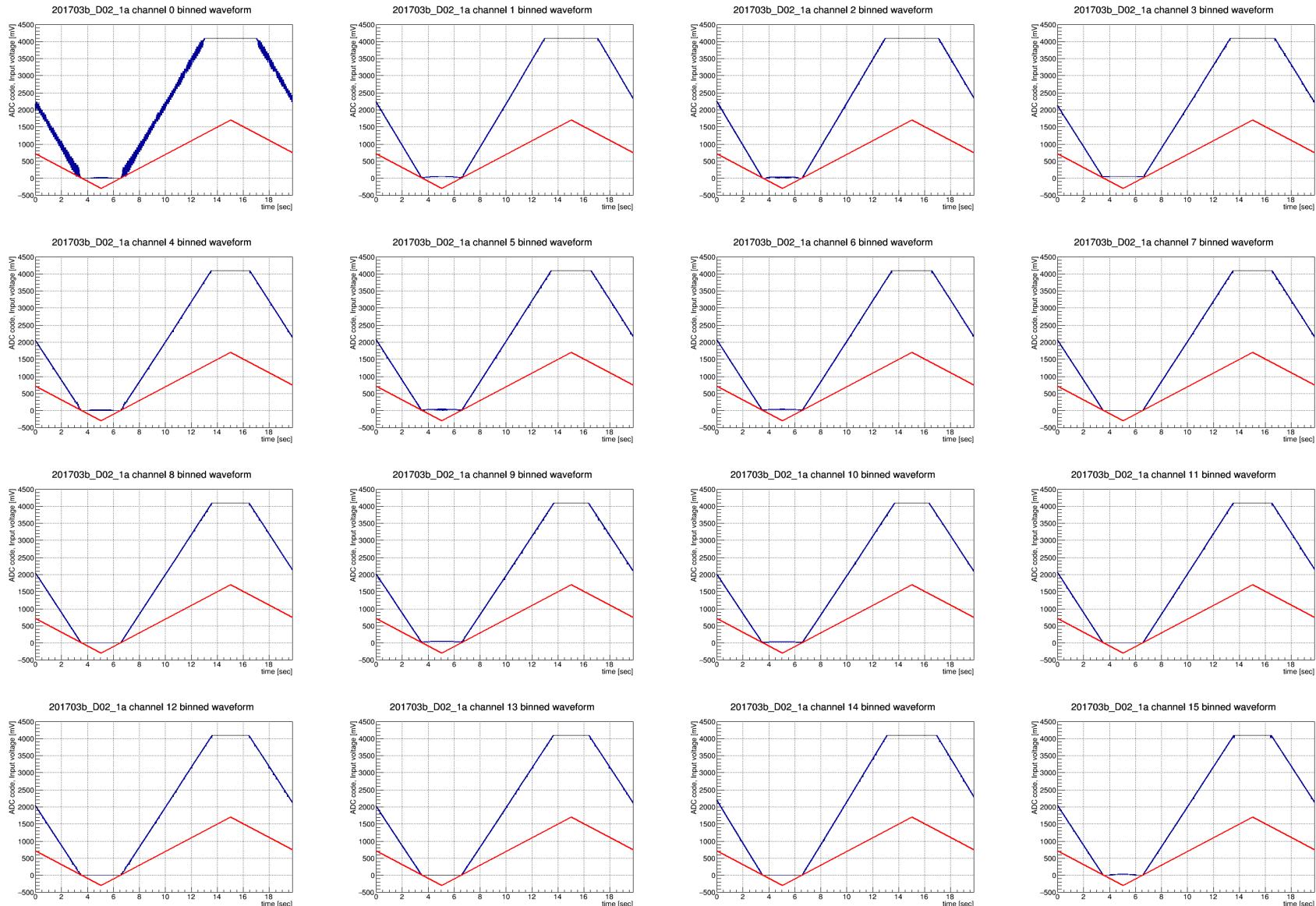
Appendix 2

Plots for all samples

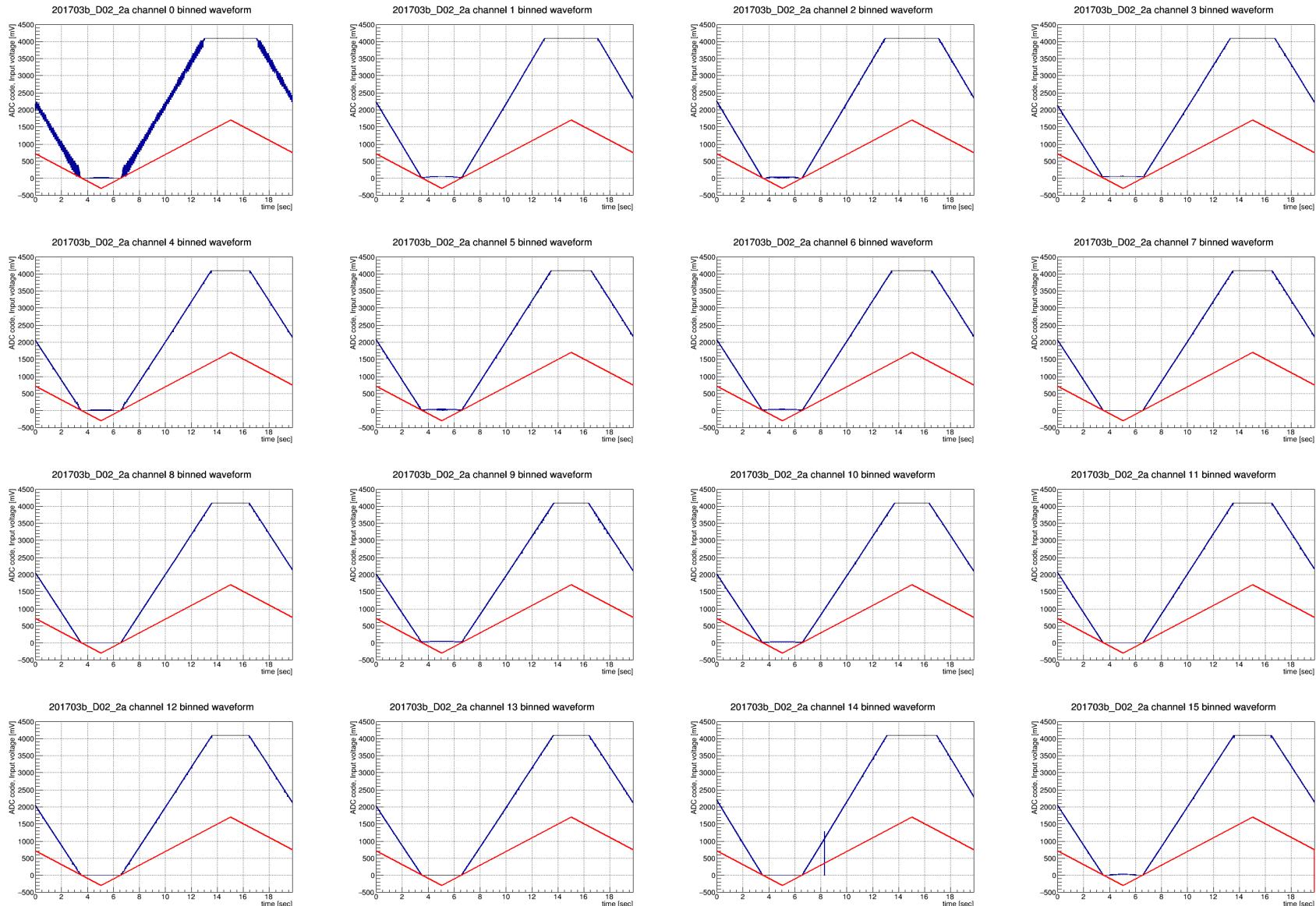
- Each page shows all channels for sample taken near the same time
- All 18 time samples for many variables:
 - Raw waveform and derived input voltage
 - Residual from linear fit
 - RMS from optimal calibration for each bin
 - Note we cut at 1 mV to identify bad channels
 - Tail fraction ($\text{RMS} > 5 \text{ mV}$)
 - Performance plots
 - Efficiency (fraction of samples not bad)
 - Resolution (RMS distribution of good samples)
 - Tail fraction
 - All in bins of input voltage

Waveforms

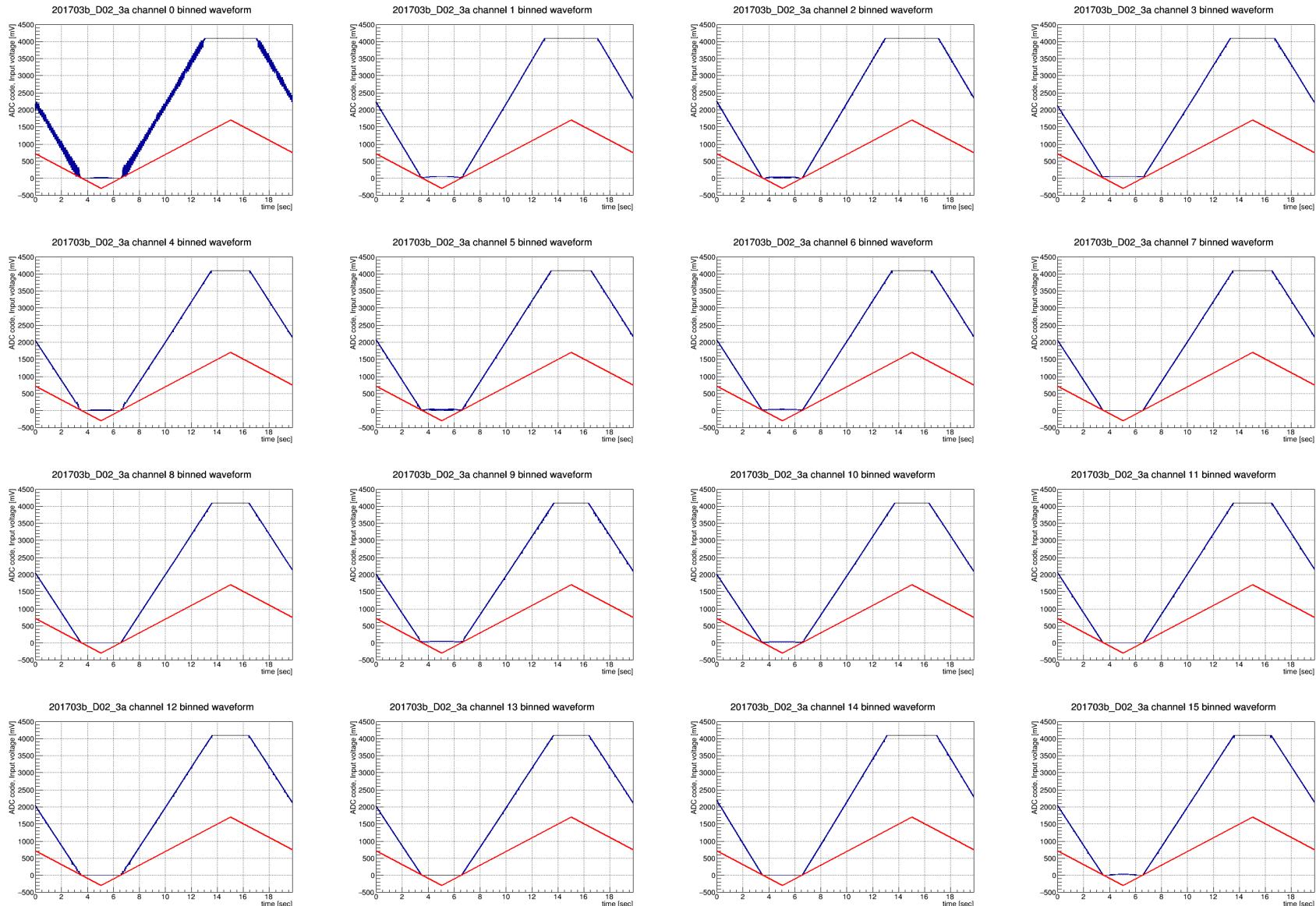
Waveforms: chip D02, time 1a



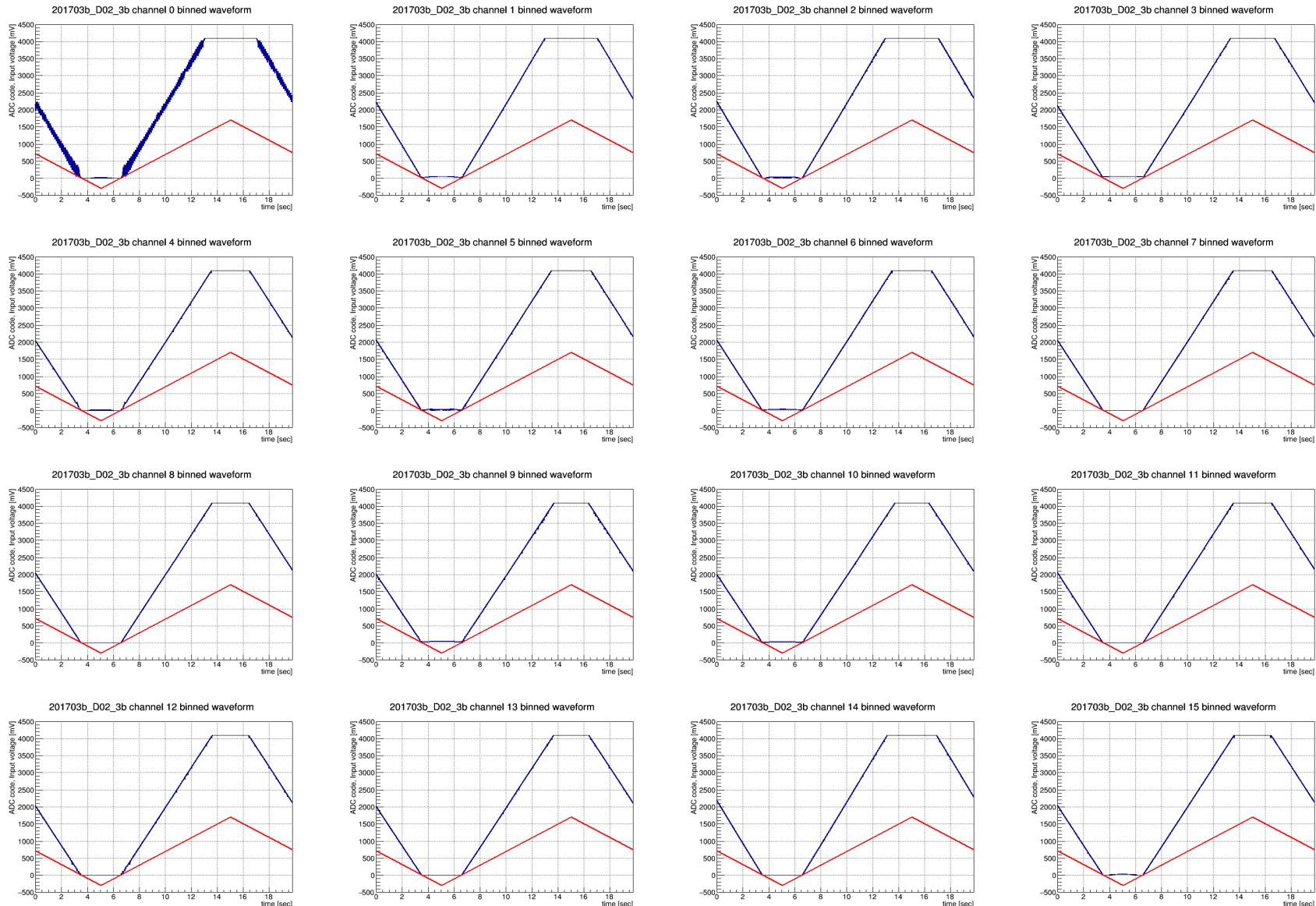
Waveforms: chip D02, time 2a



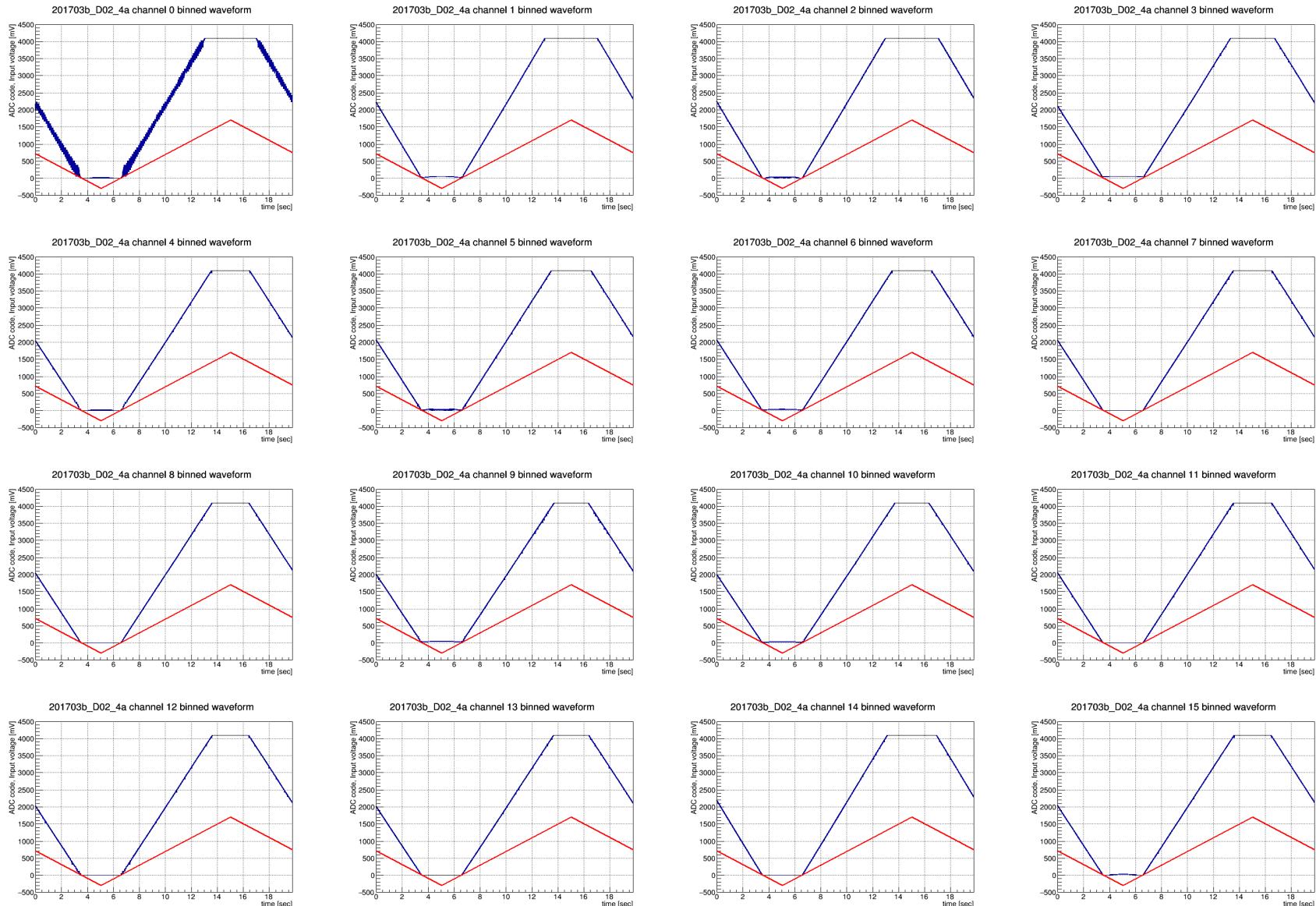
Waveforms: chip D02, time 3a



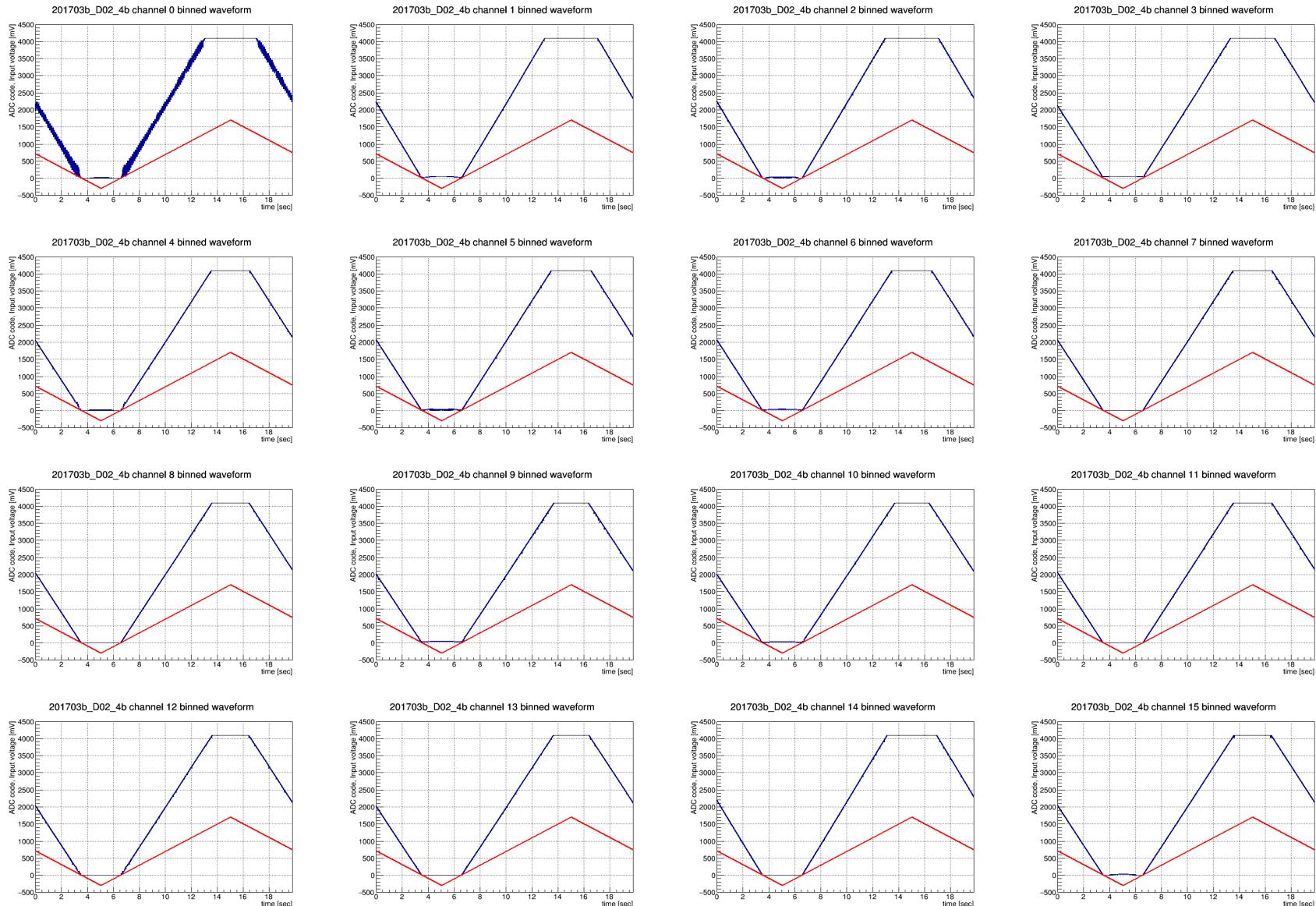
Waveforms: chip D02, time 3b



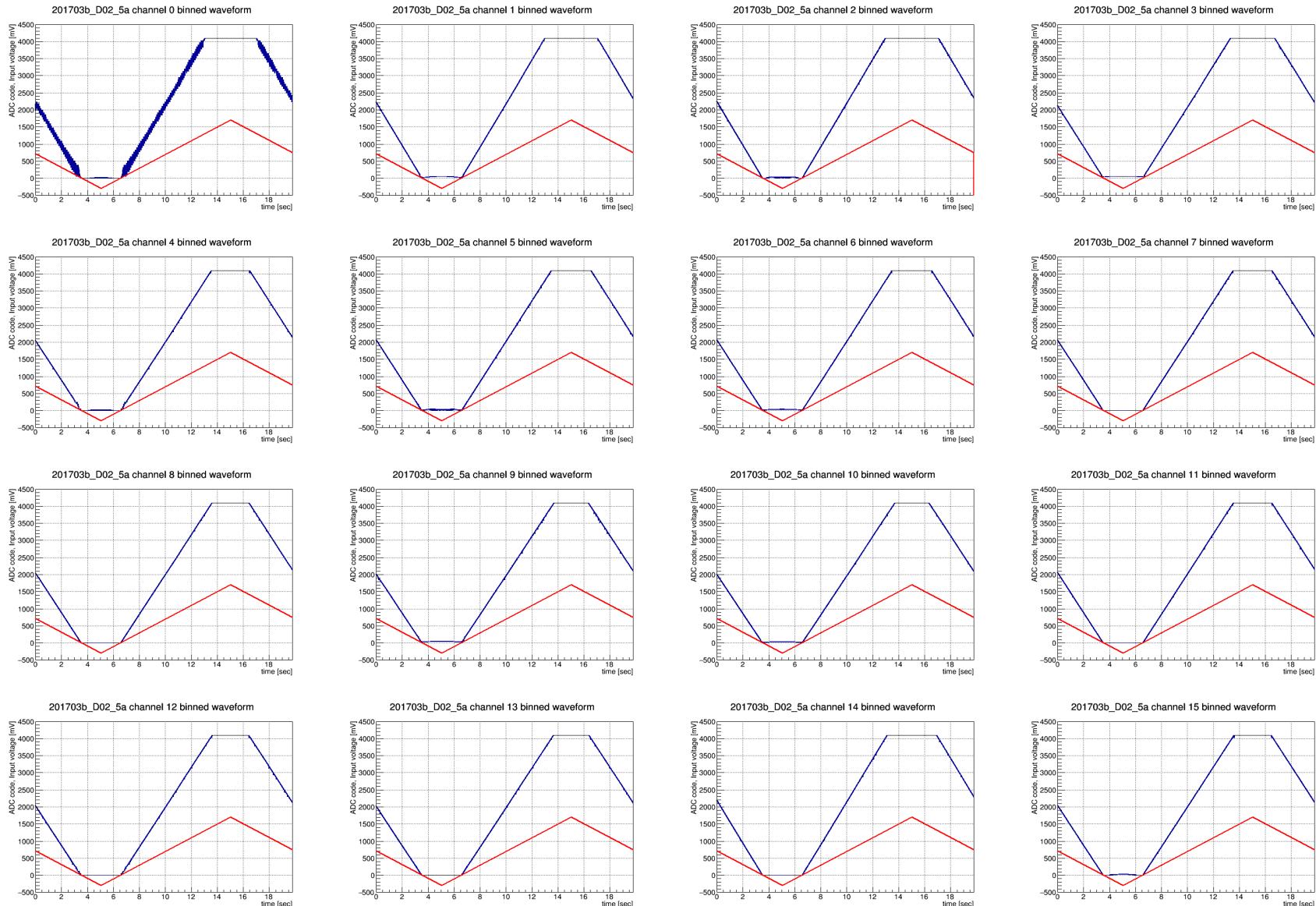
Waveforms: chip D02, time 4a



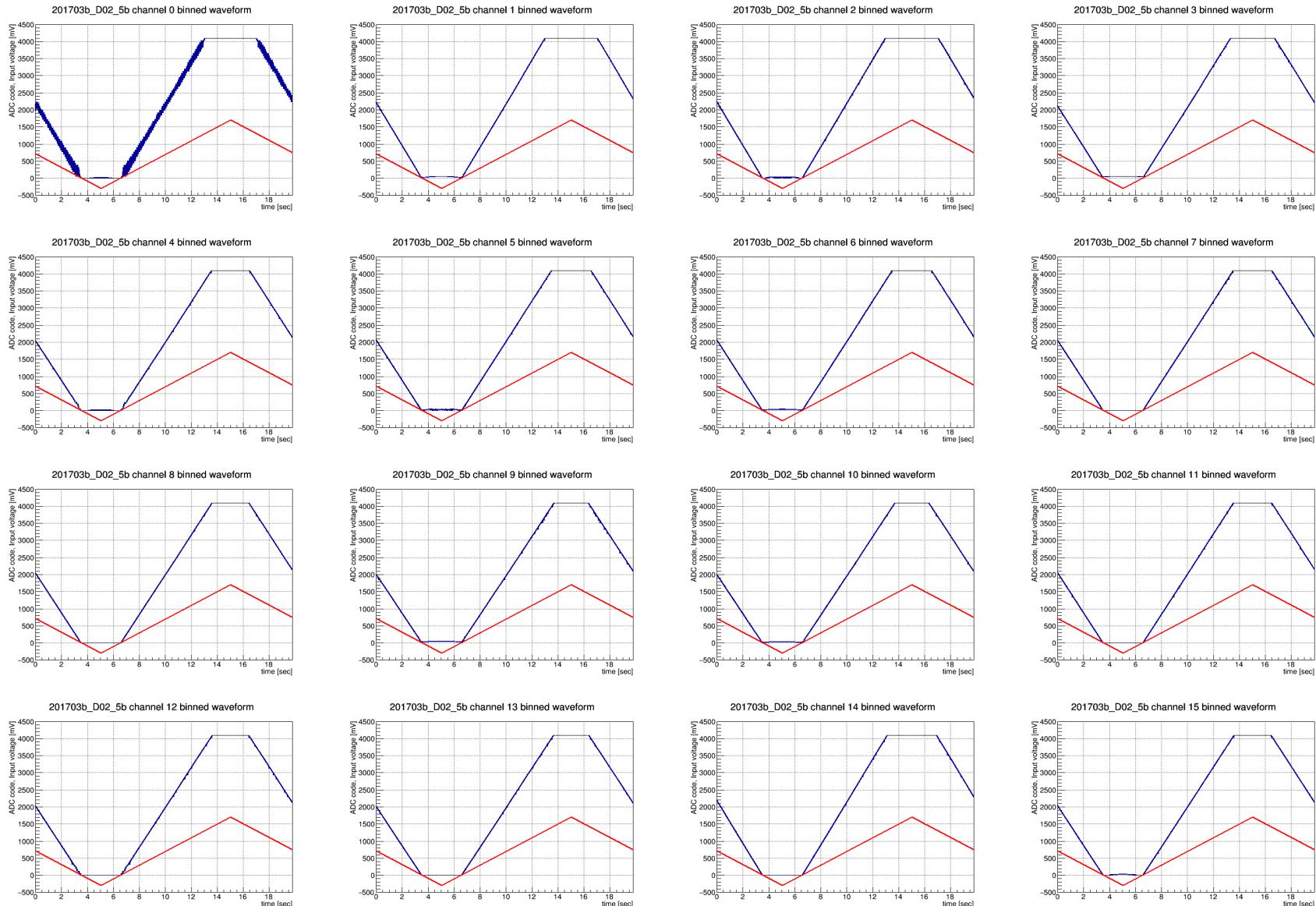
Waveforms: chip D02, time 4b



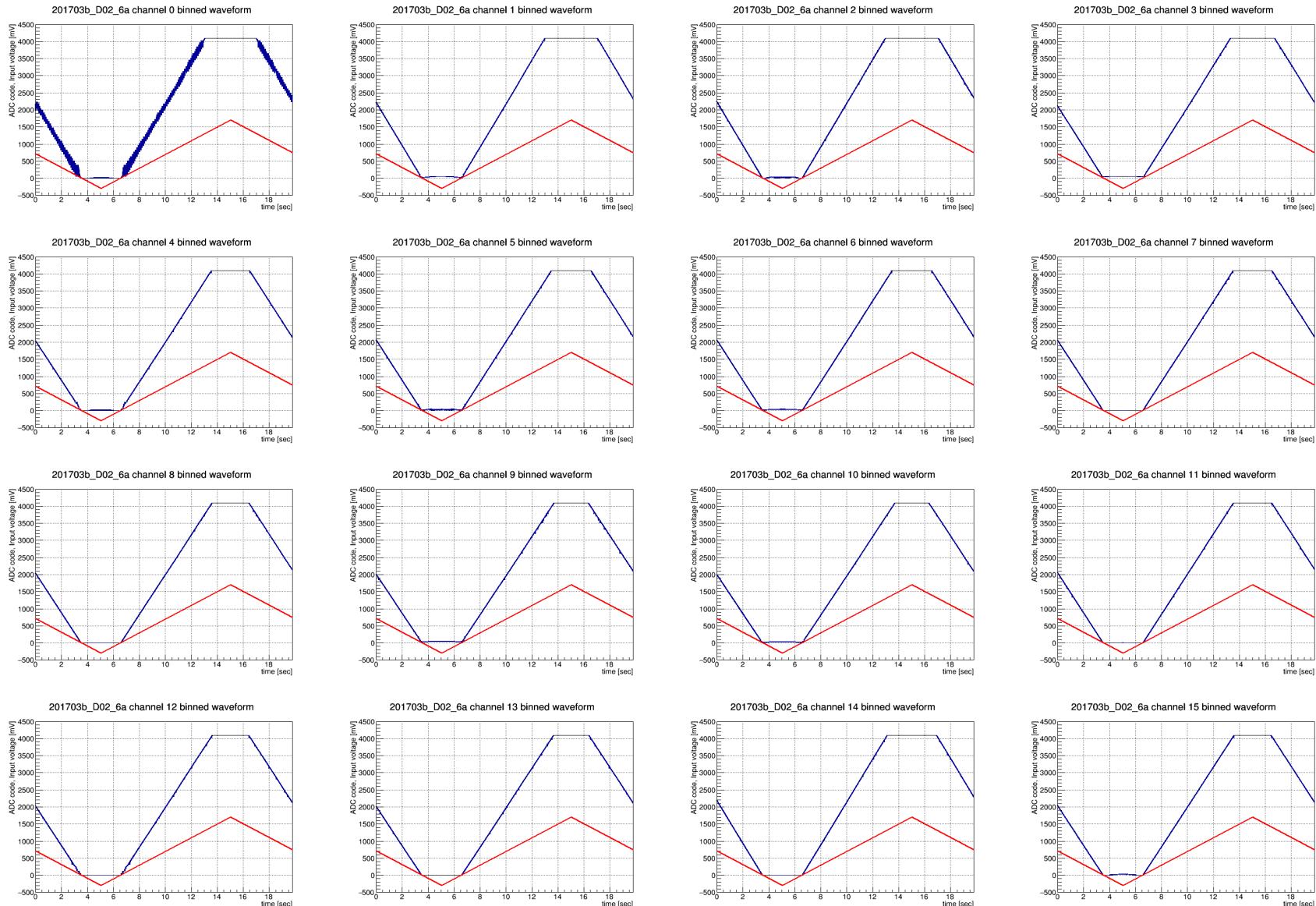
Waveforms: chip D02, time 5a



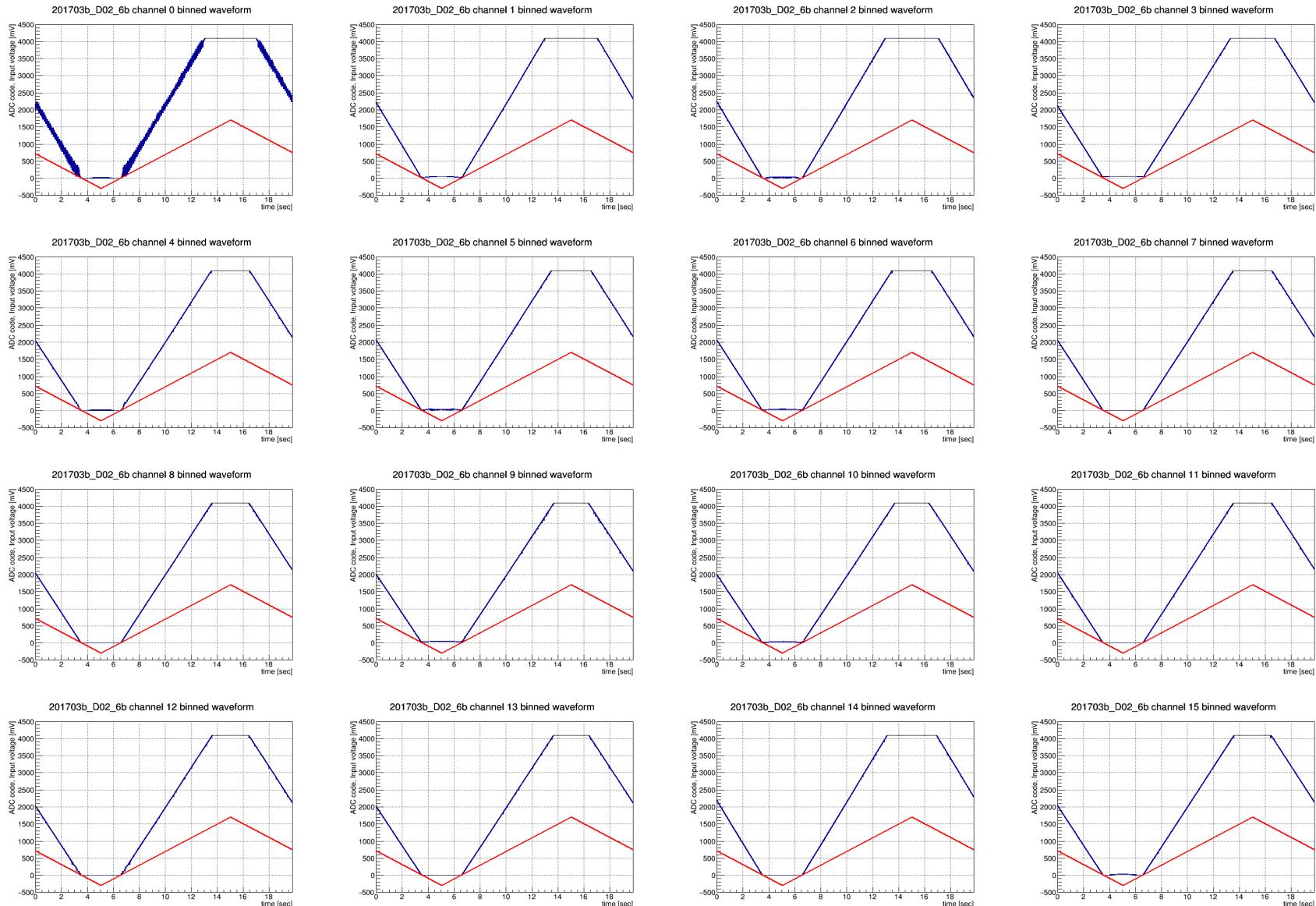
Waveforms: chip D02, time 5b



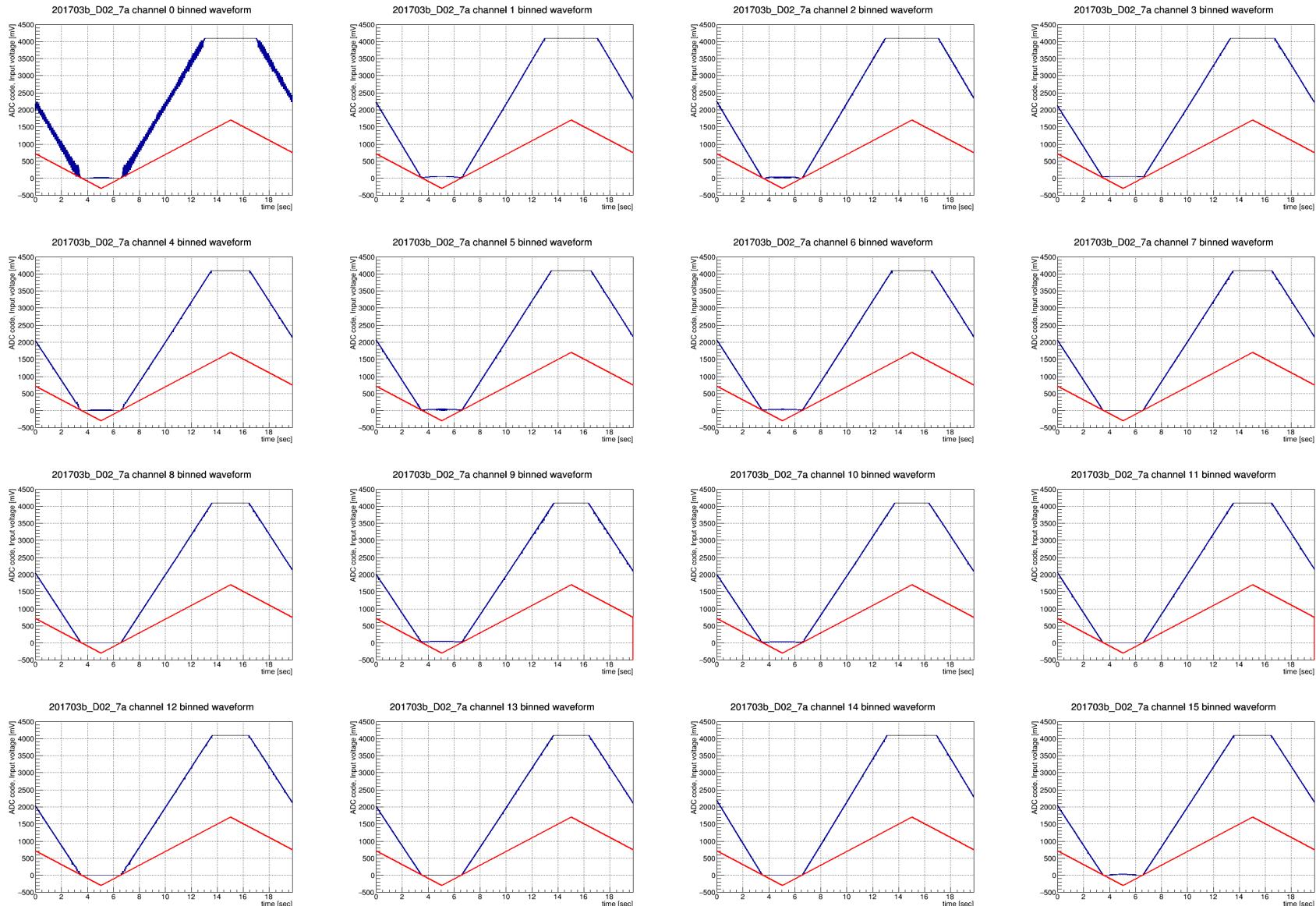
Waveforms: chip D02, time 6a



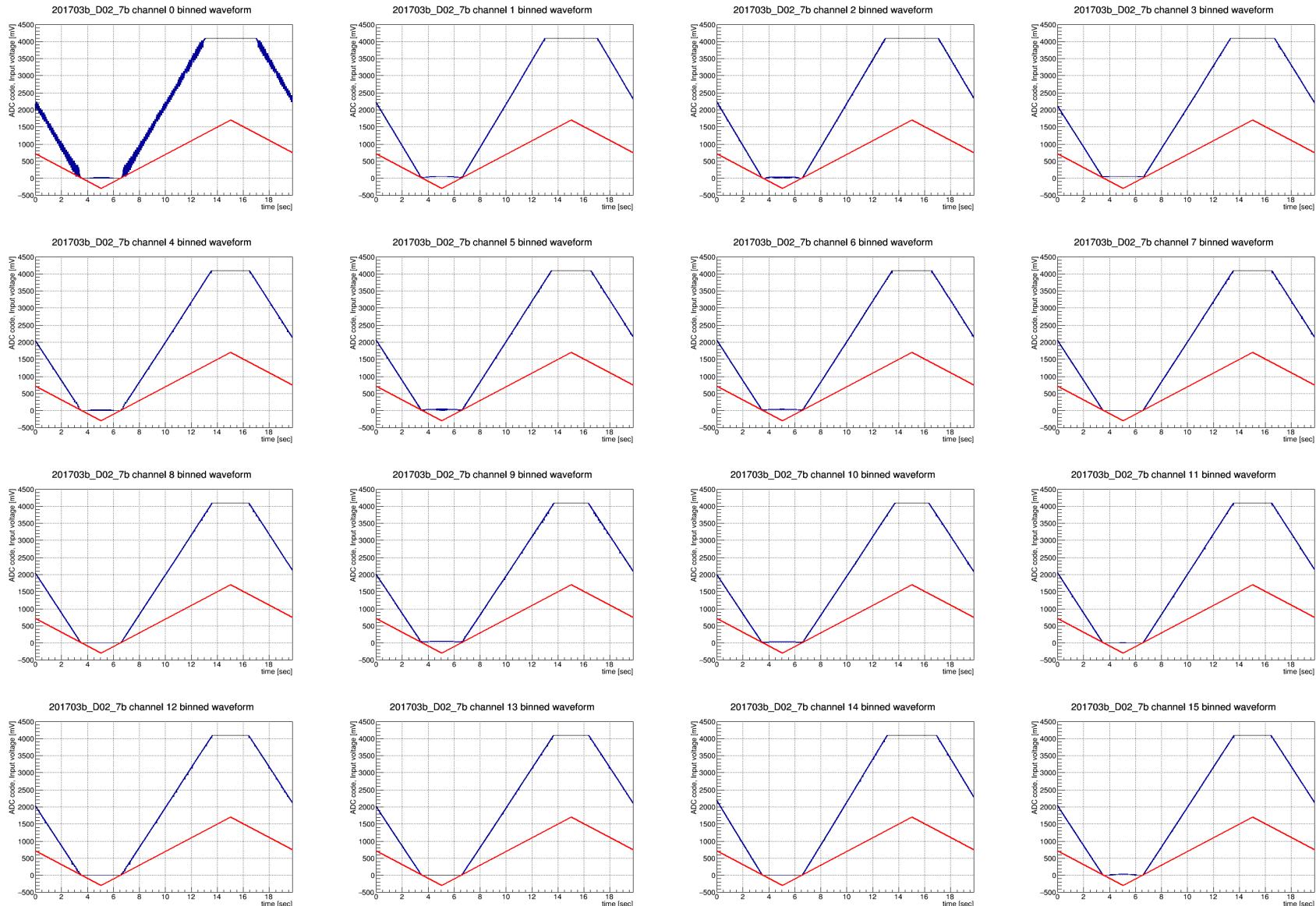
Waveforms: chip D02, time 6b



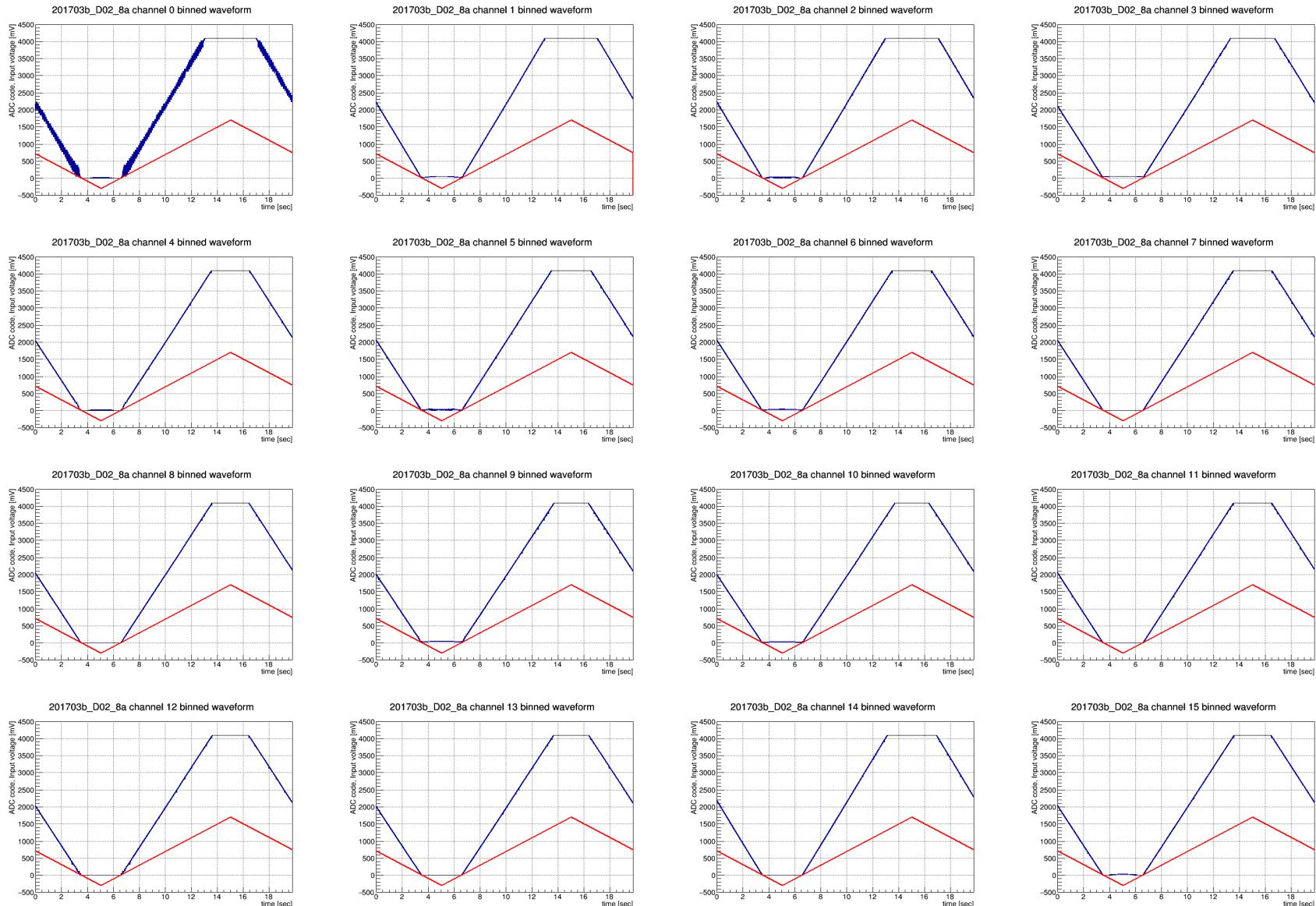
Waveforms: chip D02, time 7a



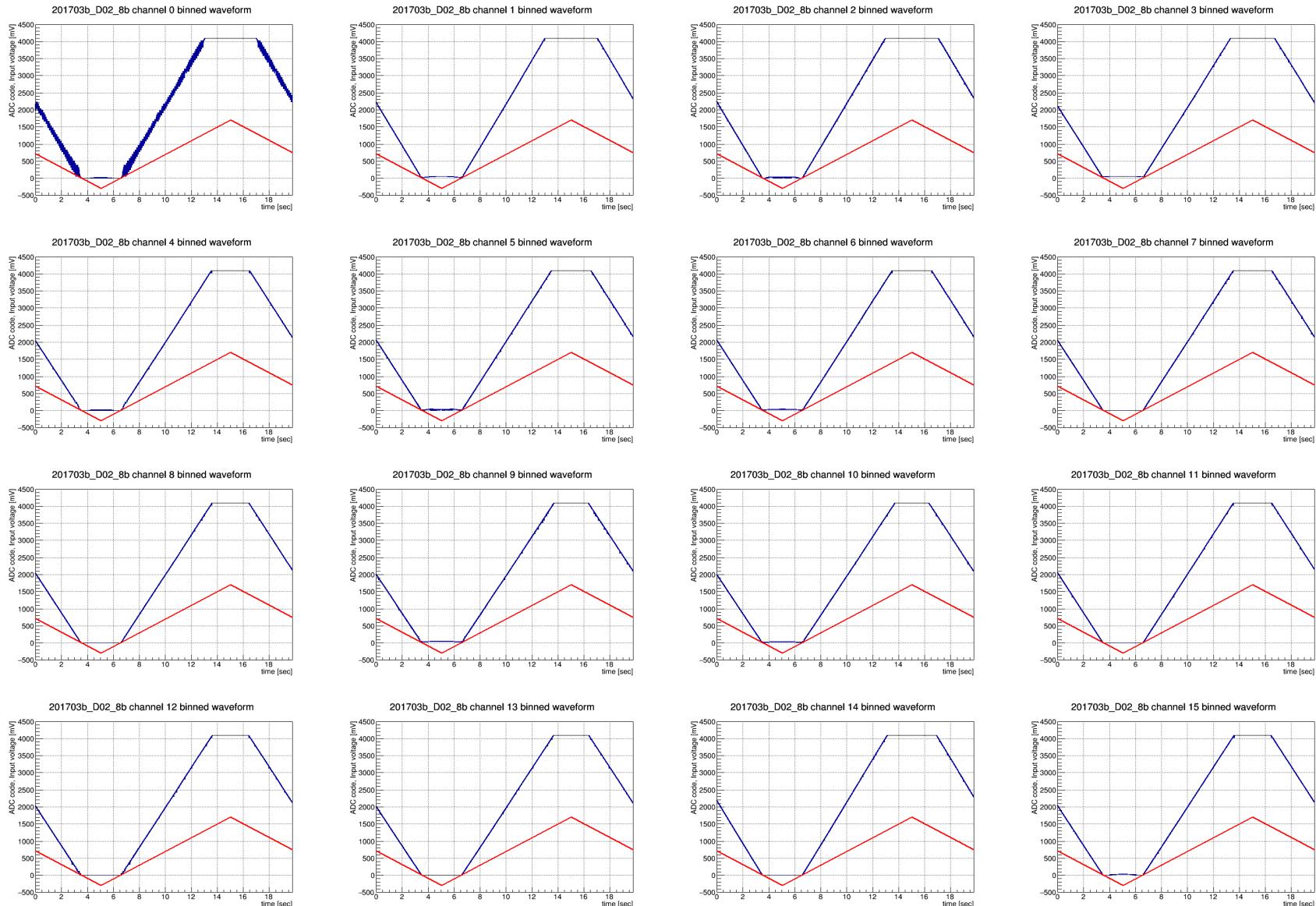
Waveforms: chip D02, time 7b



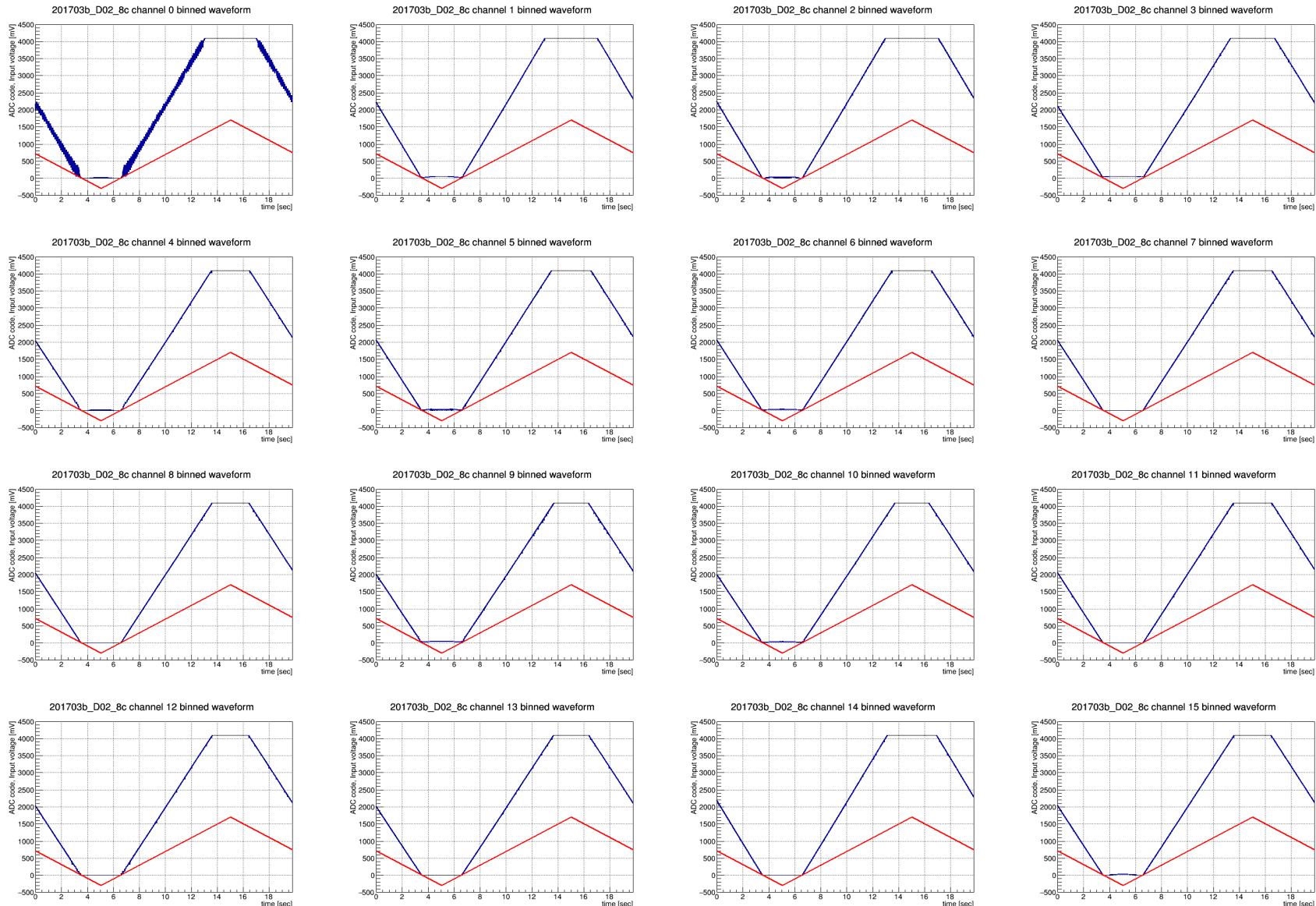
Waveforms: chip D02, time 8a



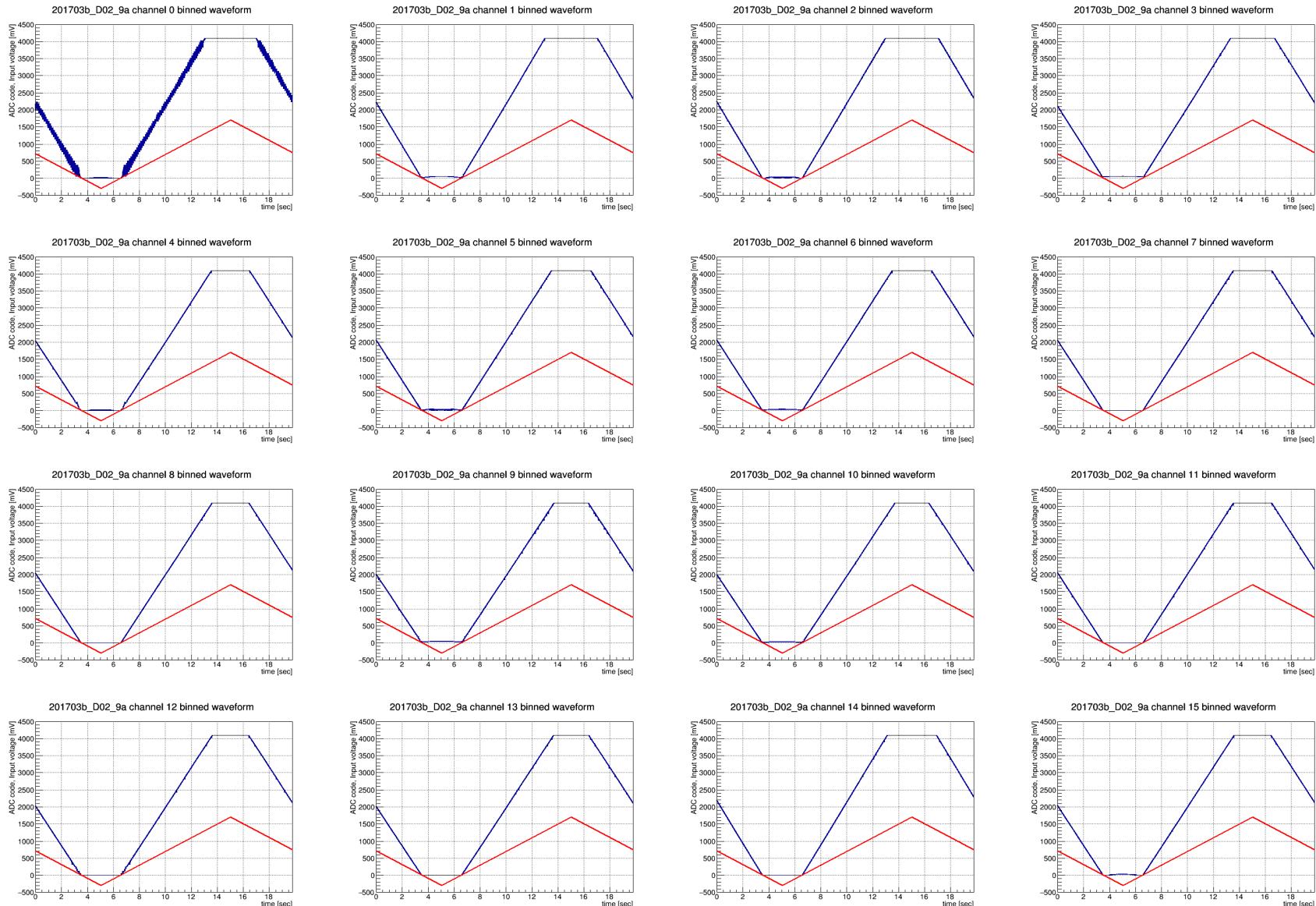
Waveforms: chip D02, time 8b



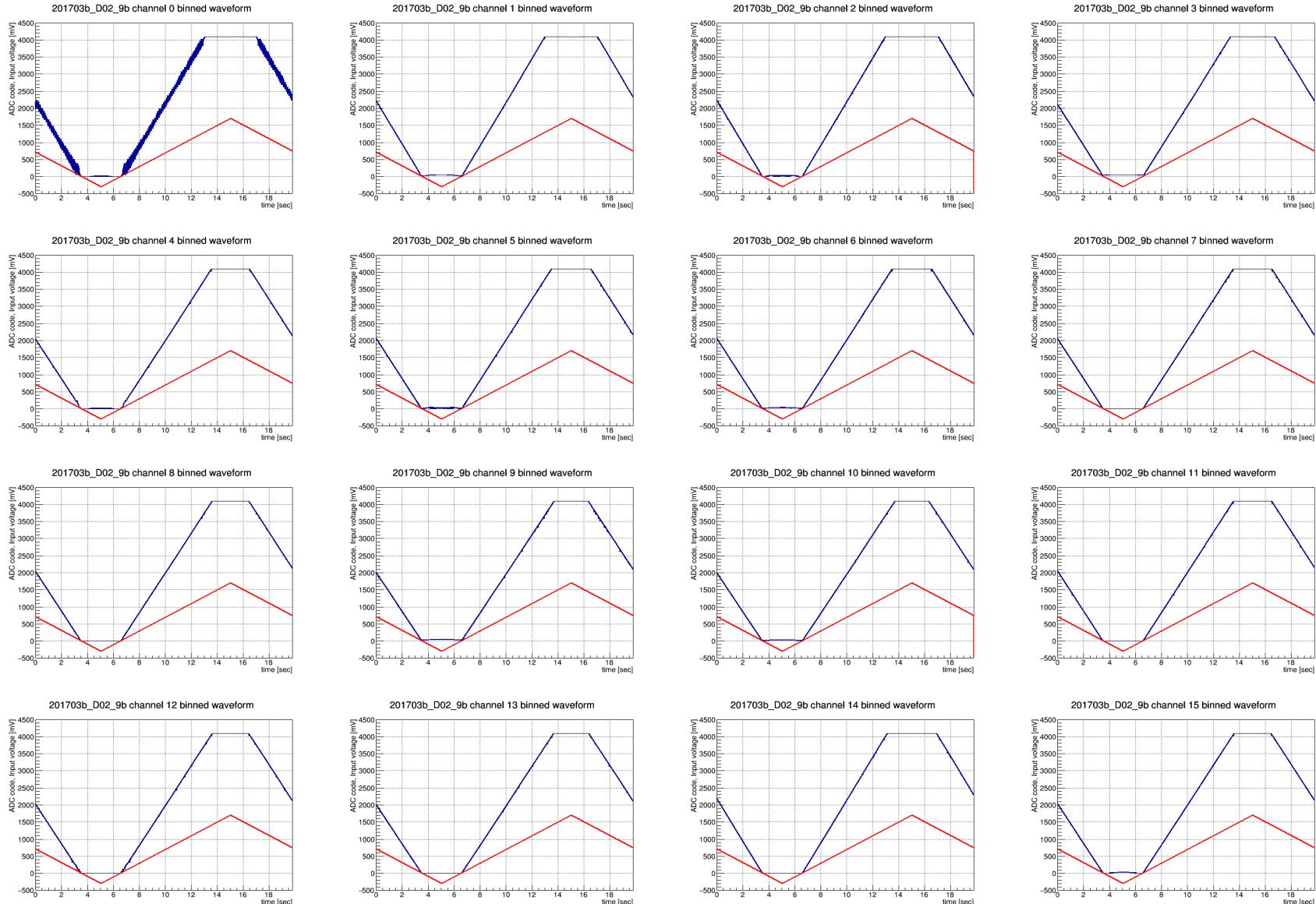
Waveforms: chip D02, time 8c



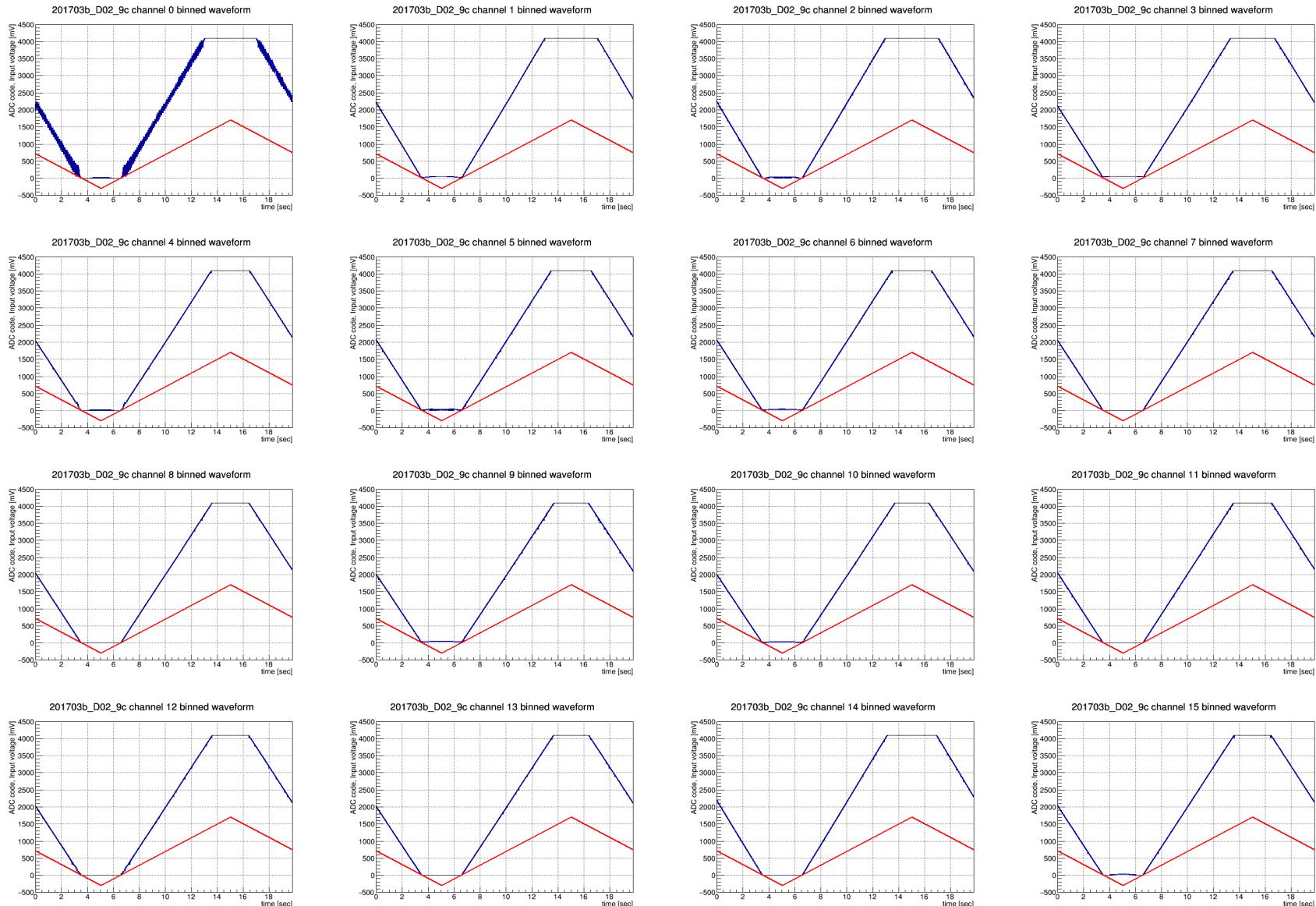
Waveforms: chip D02, time 9a



Waveforms: chip D02, time 9b

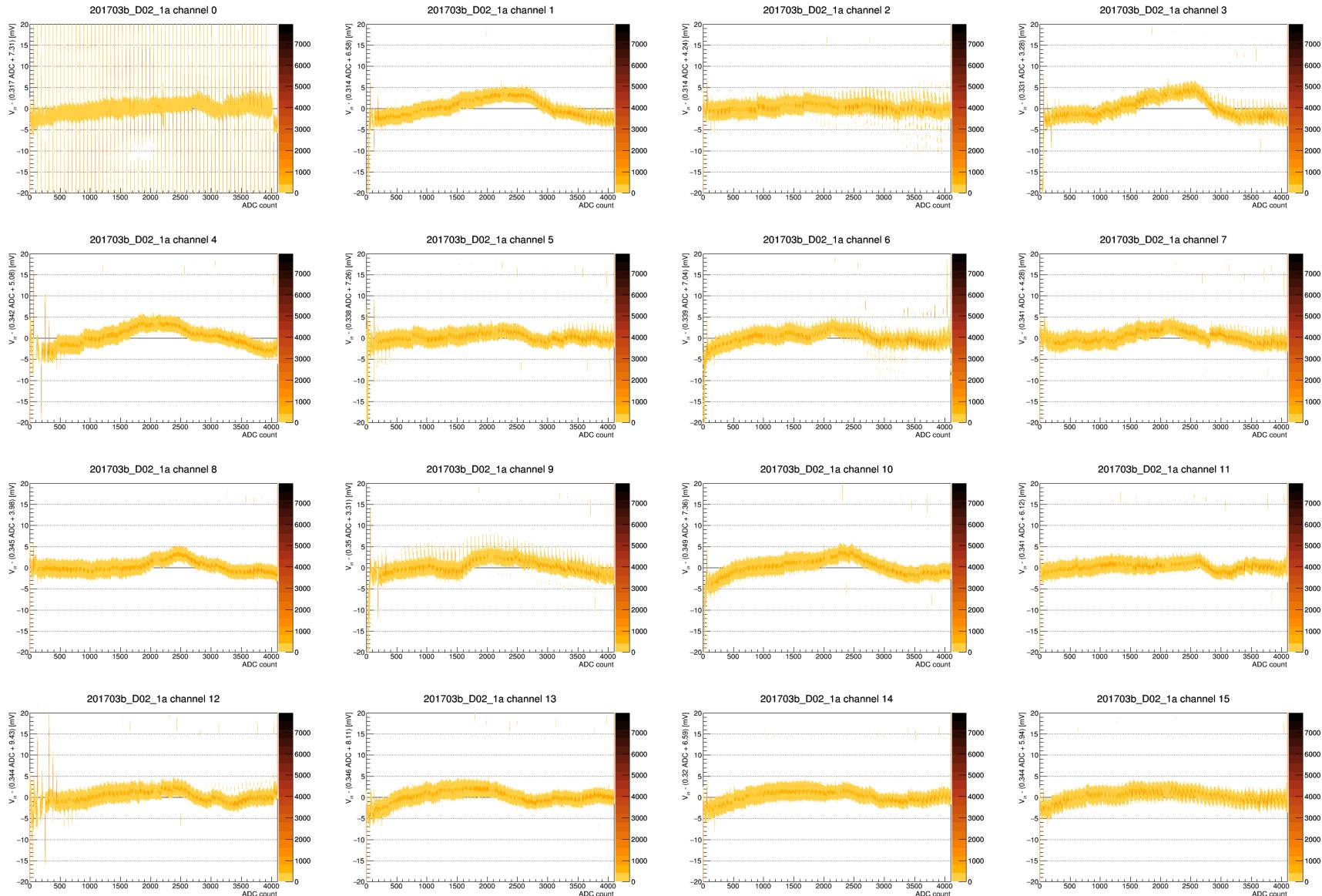


Waveforms: chip D02, time 9c

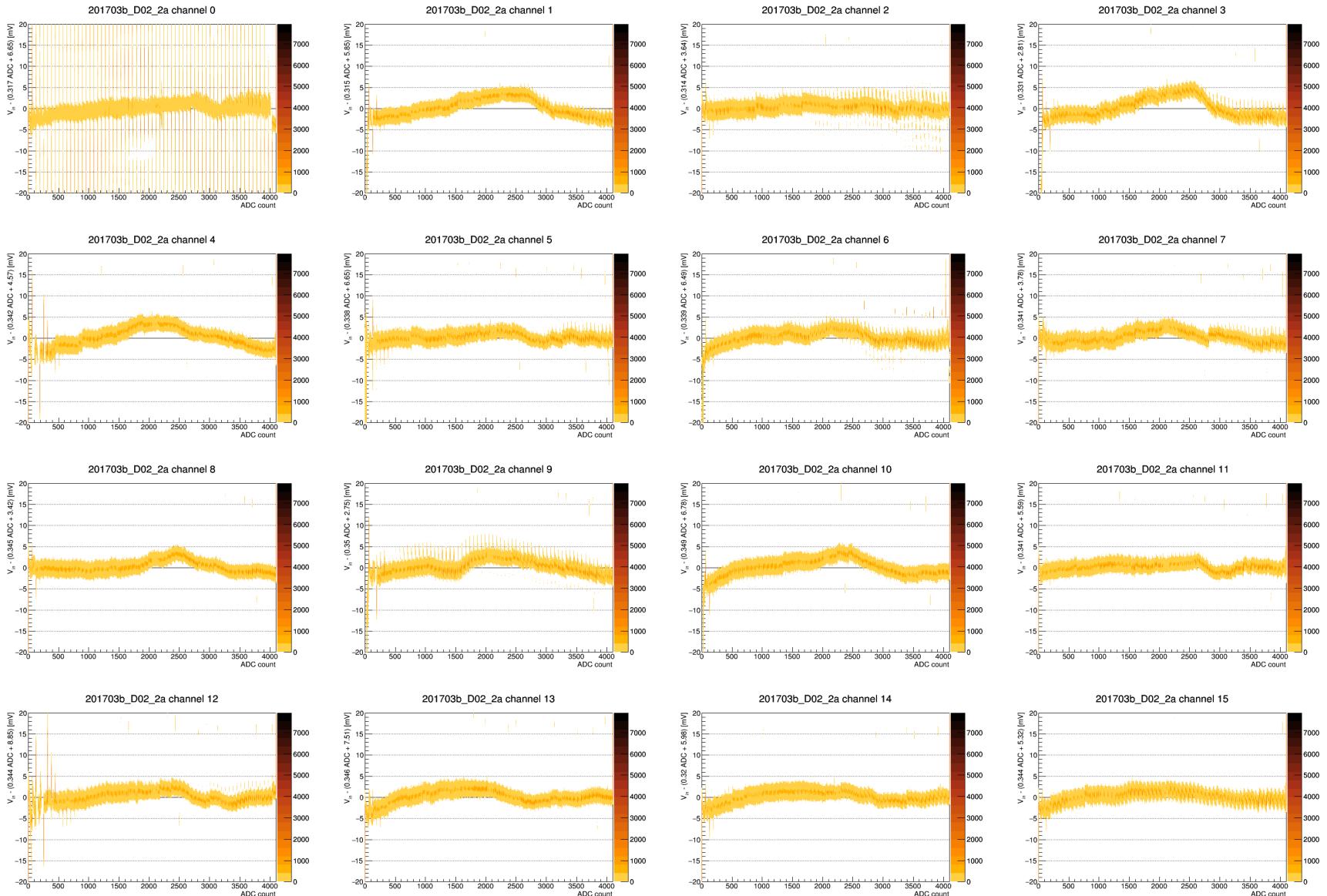


Residuals

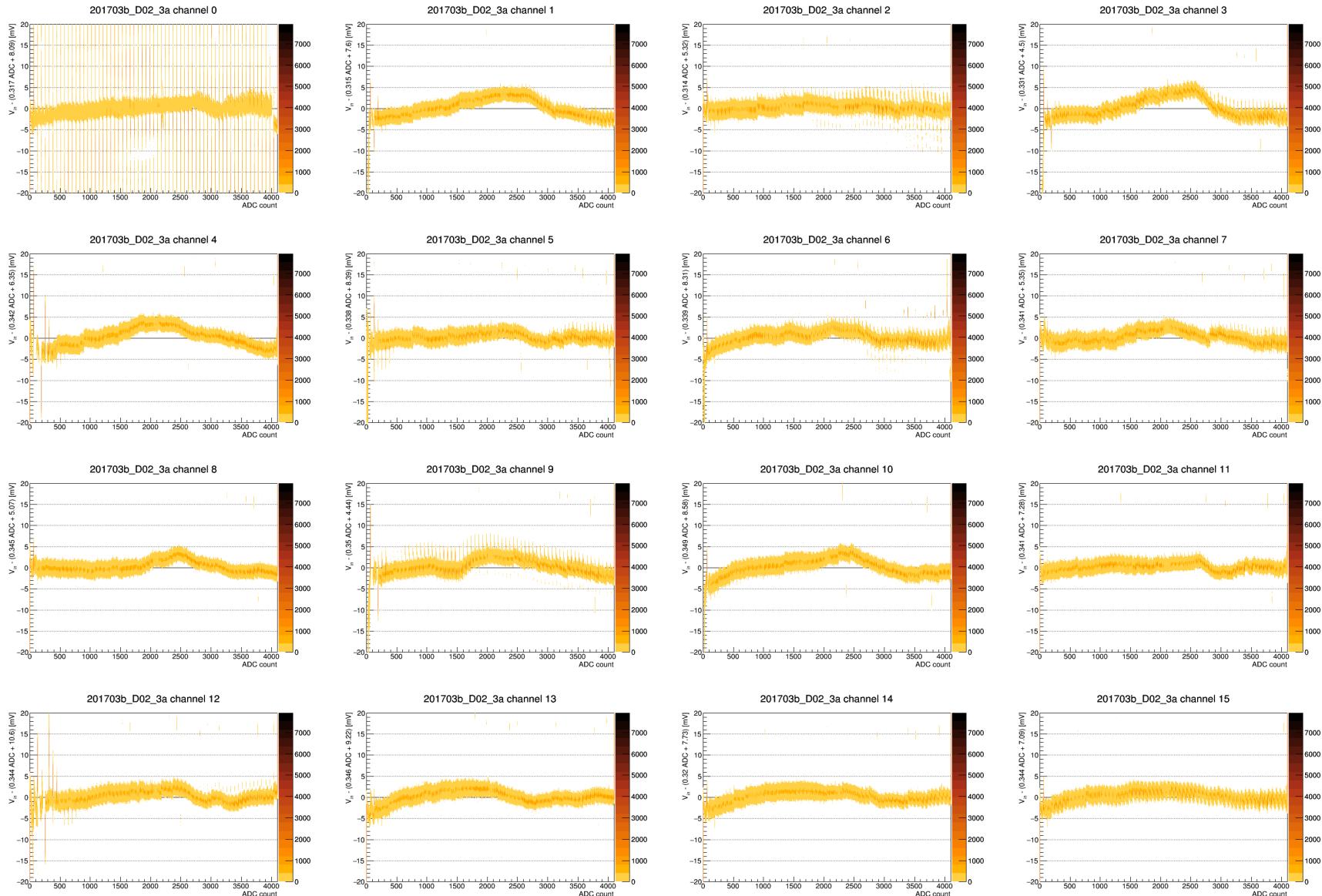
Residuals: chip D02, time 1a



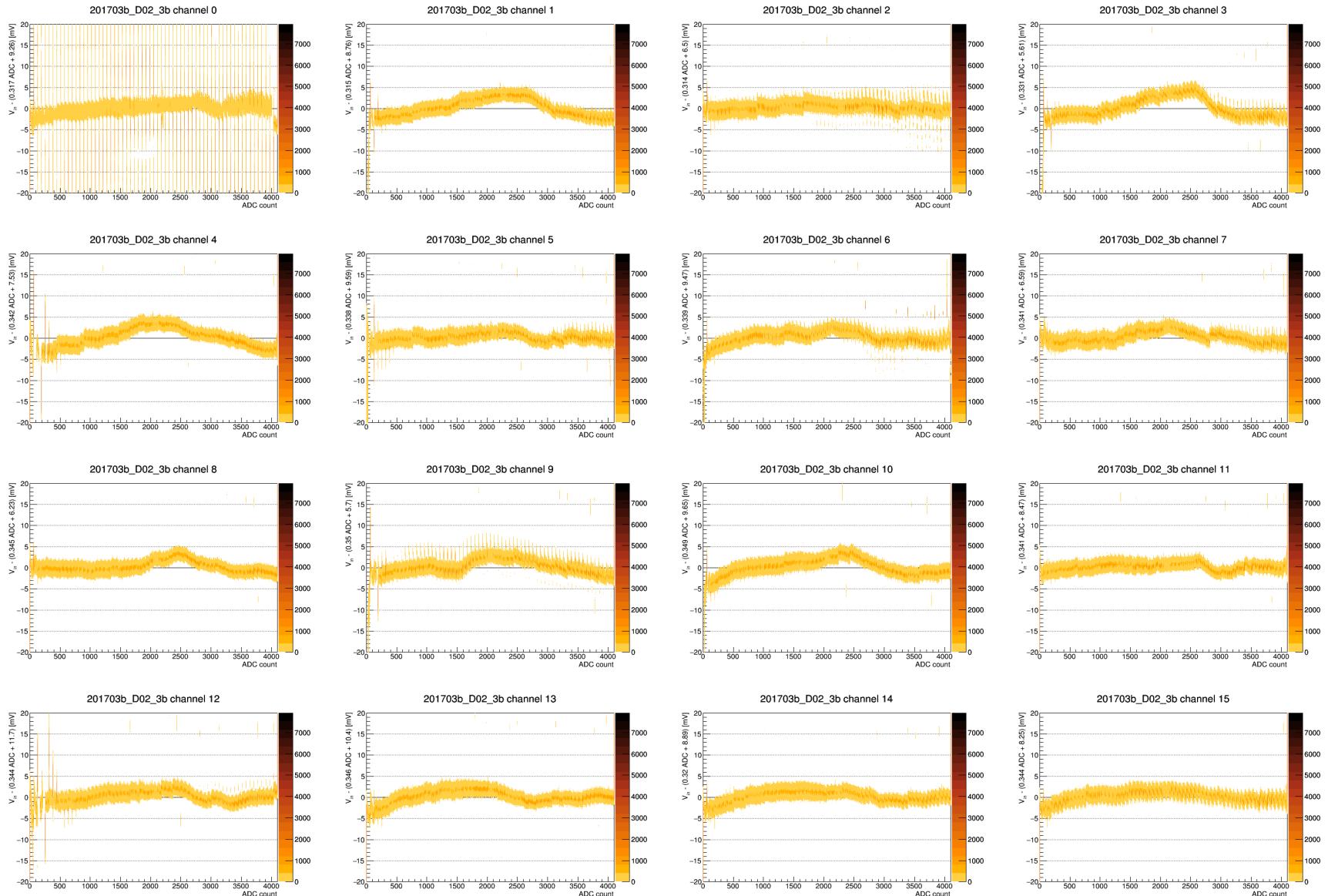
Residuals: chip D02, time 2a



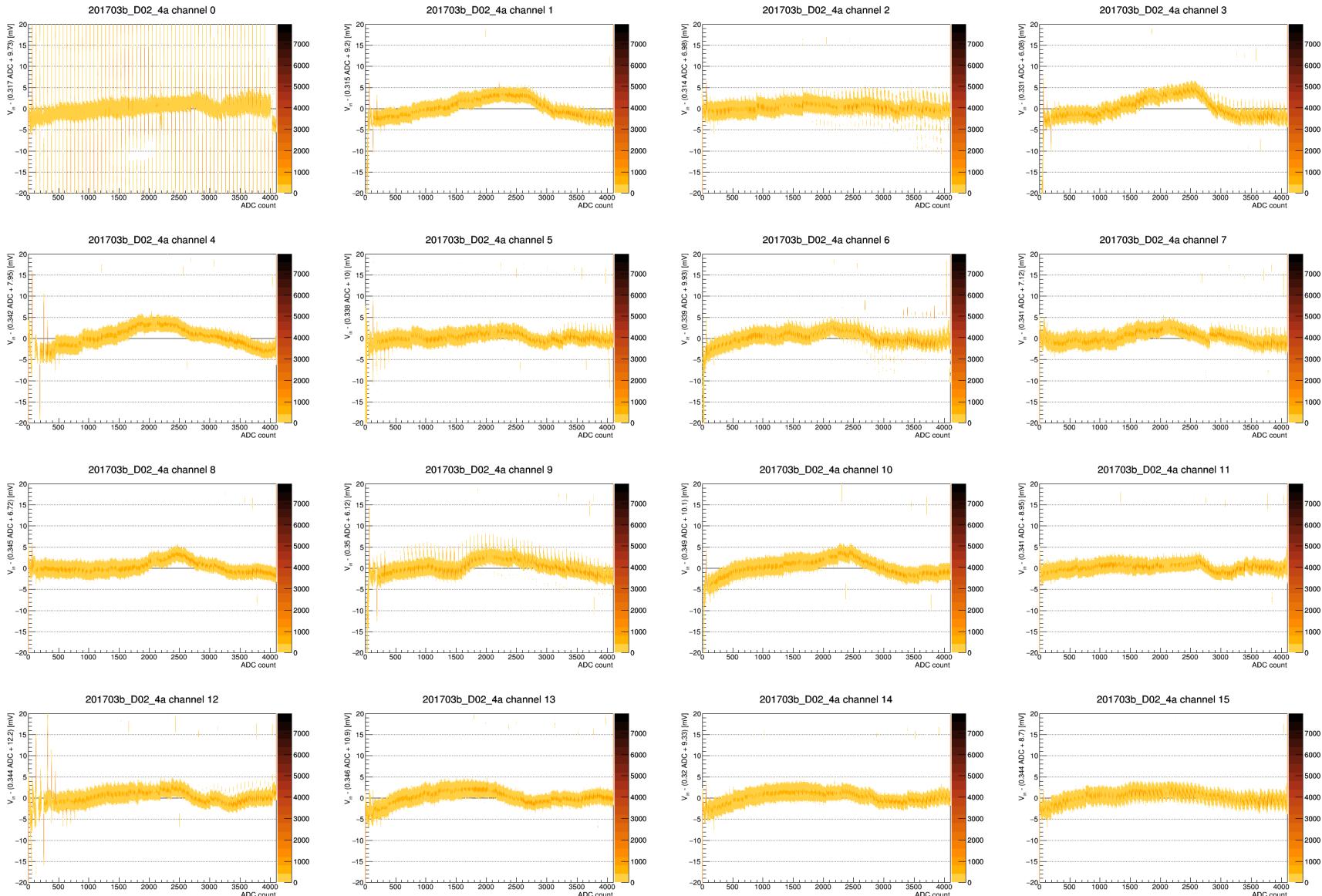
Residuals: chip D02, time 3a



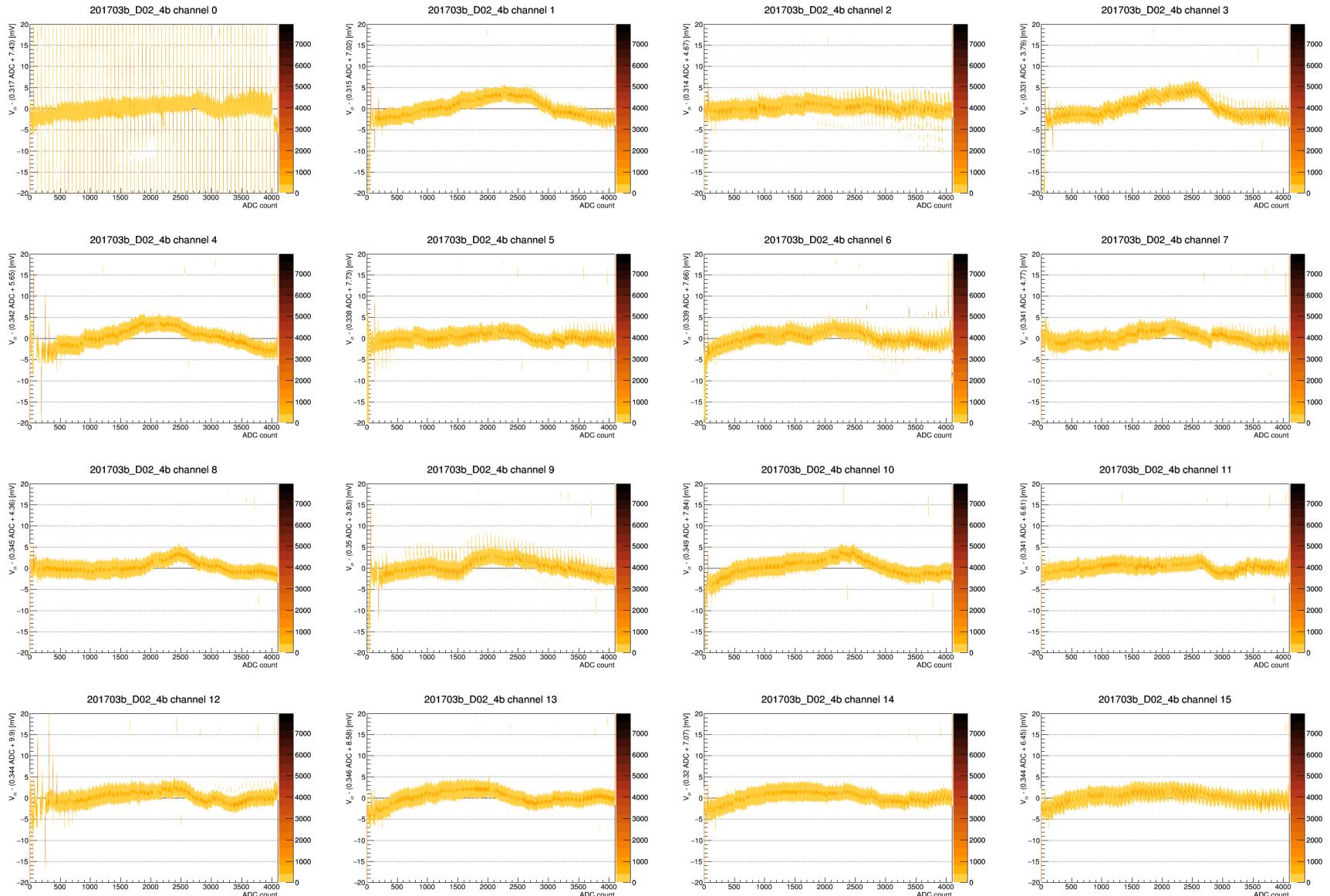
Residuals: chip D02, time 3b



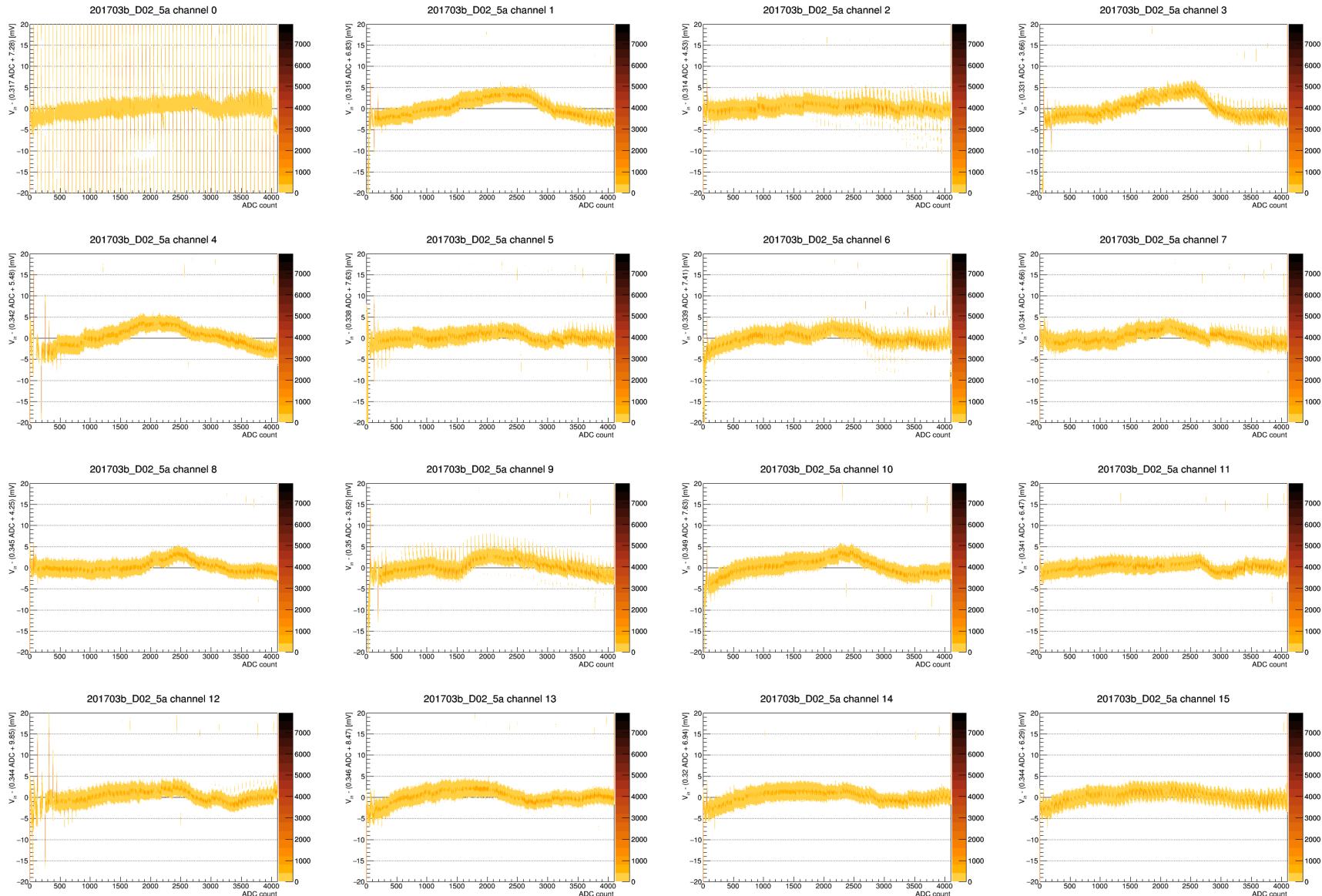
Residuals: chip D02, time 4a



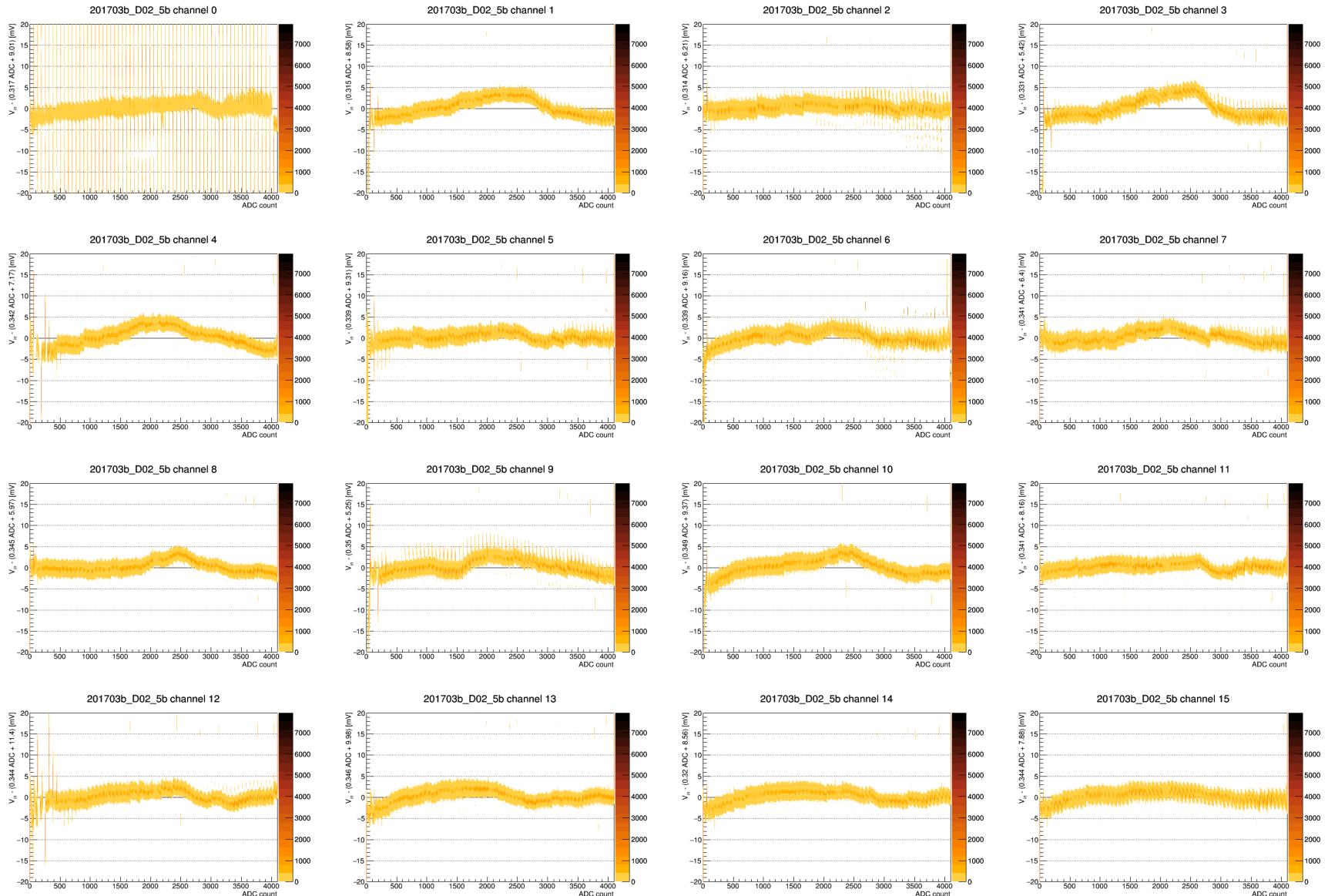
Residuals: chip D02, time 4b



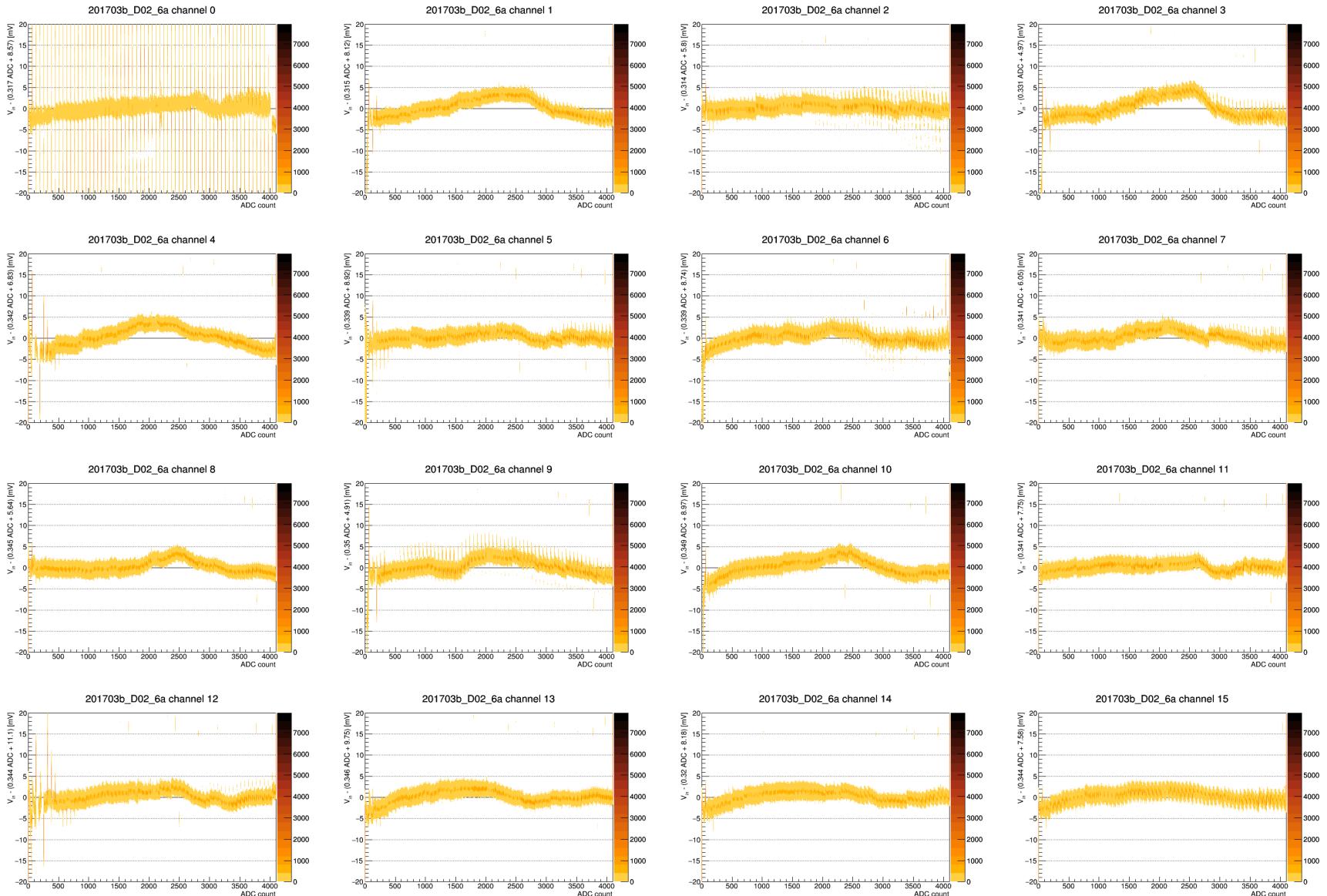
Residuals: chip D02, time 5a



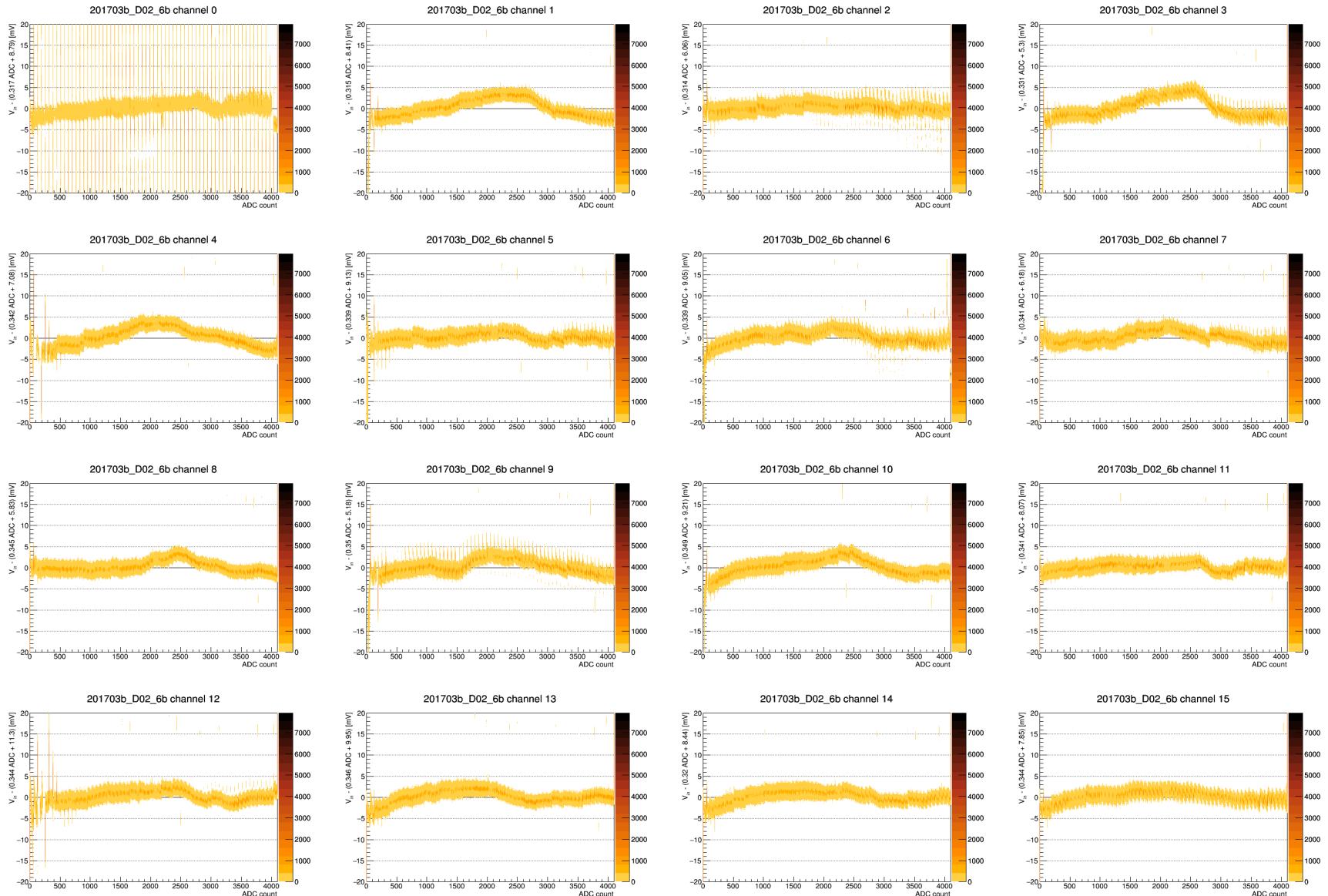
Residuals: chip D02, time 5b



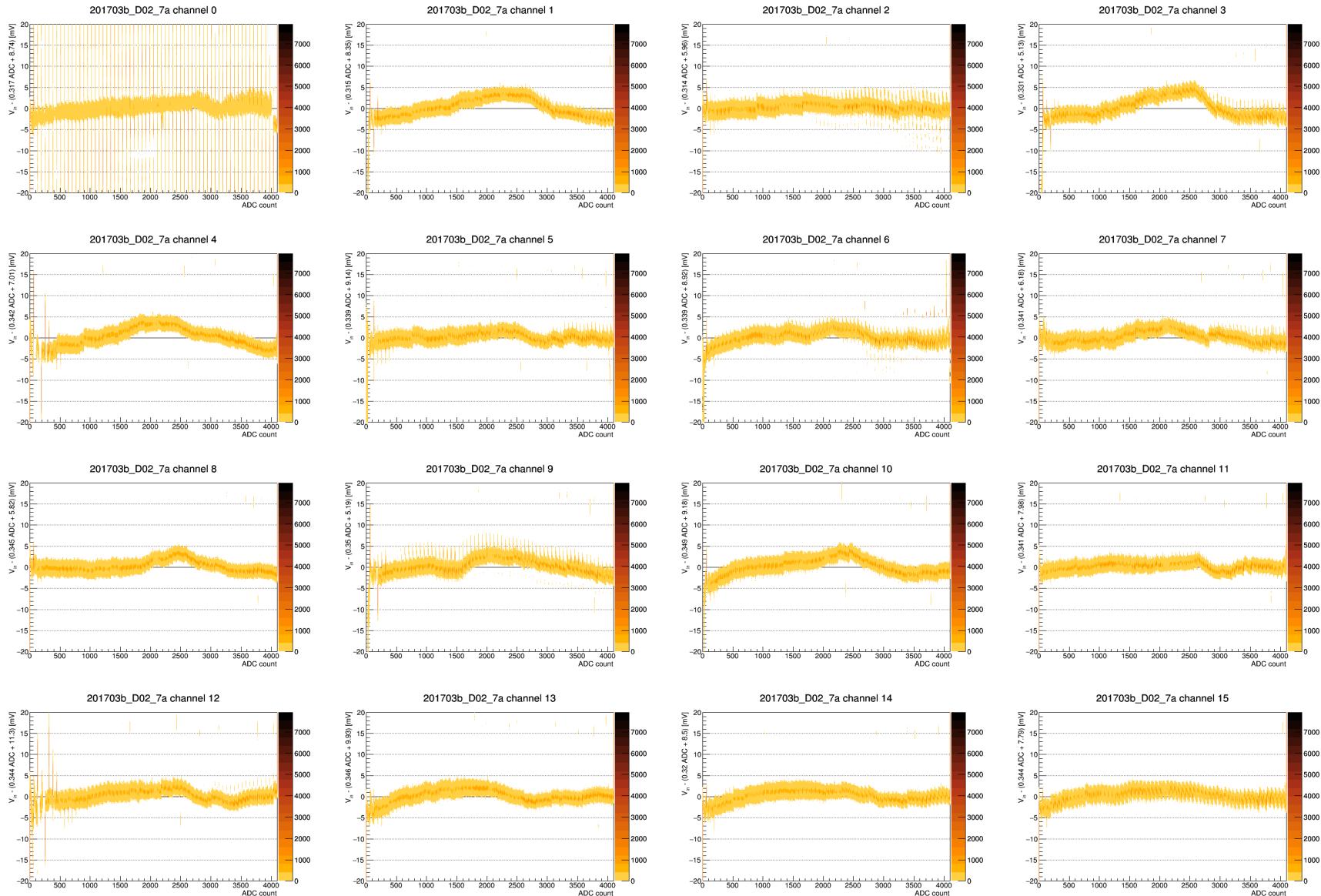
Residuals: chip D02, time 6a



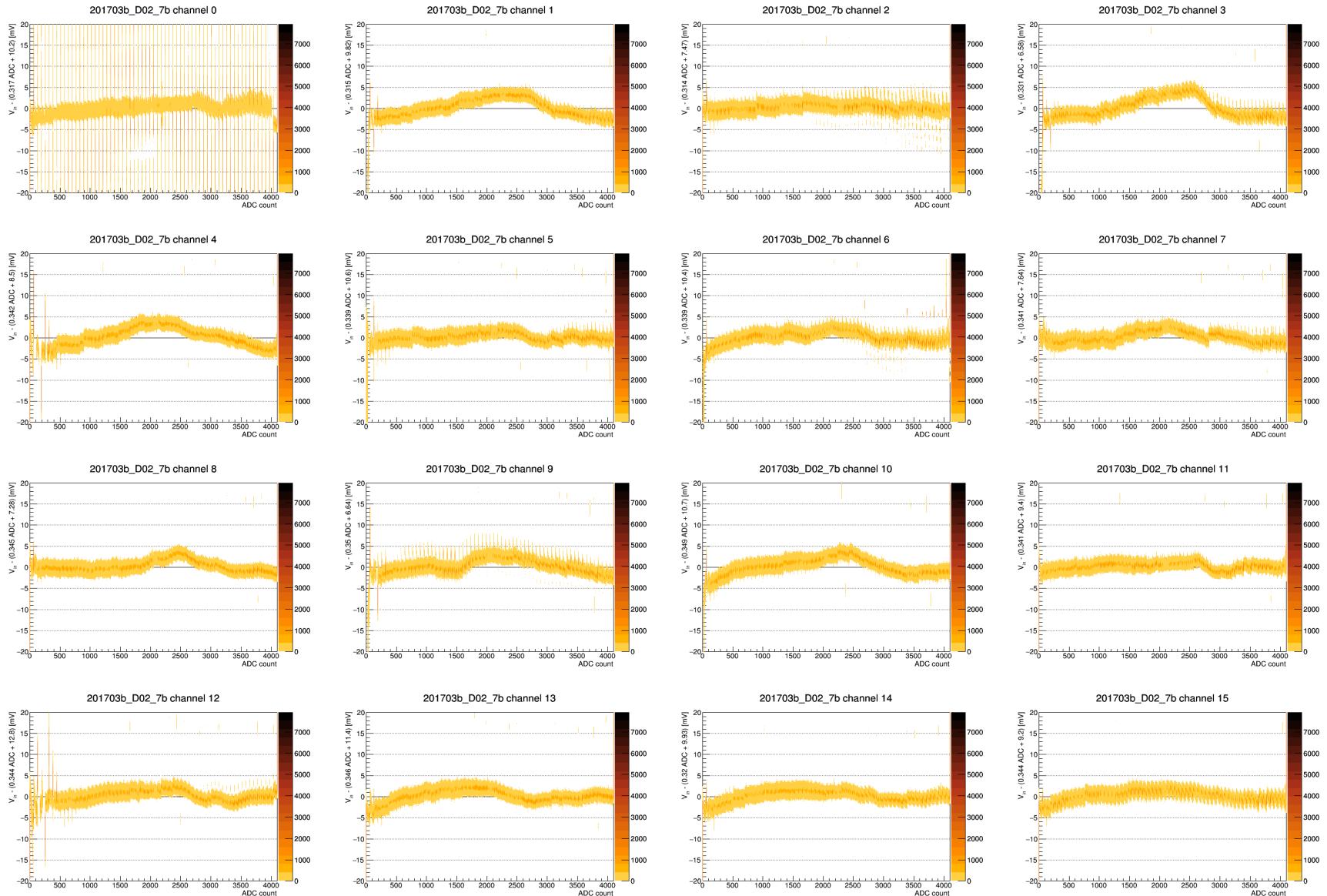
Residuals: chip D02, time 6b



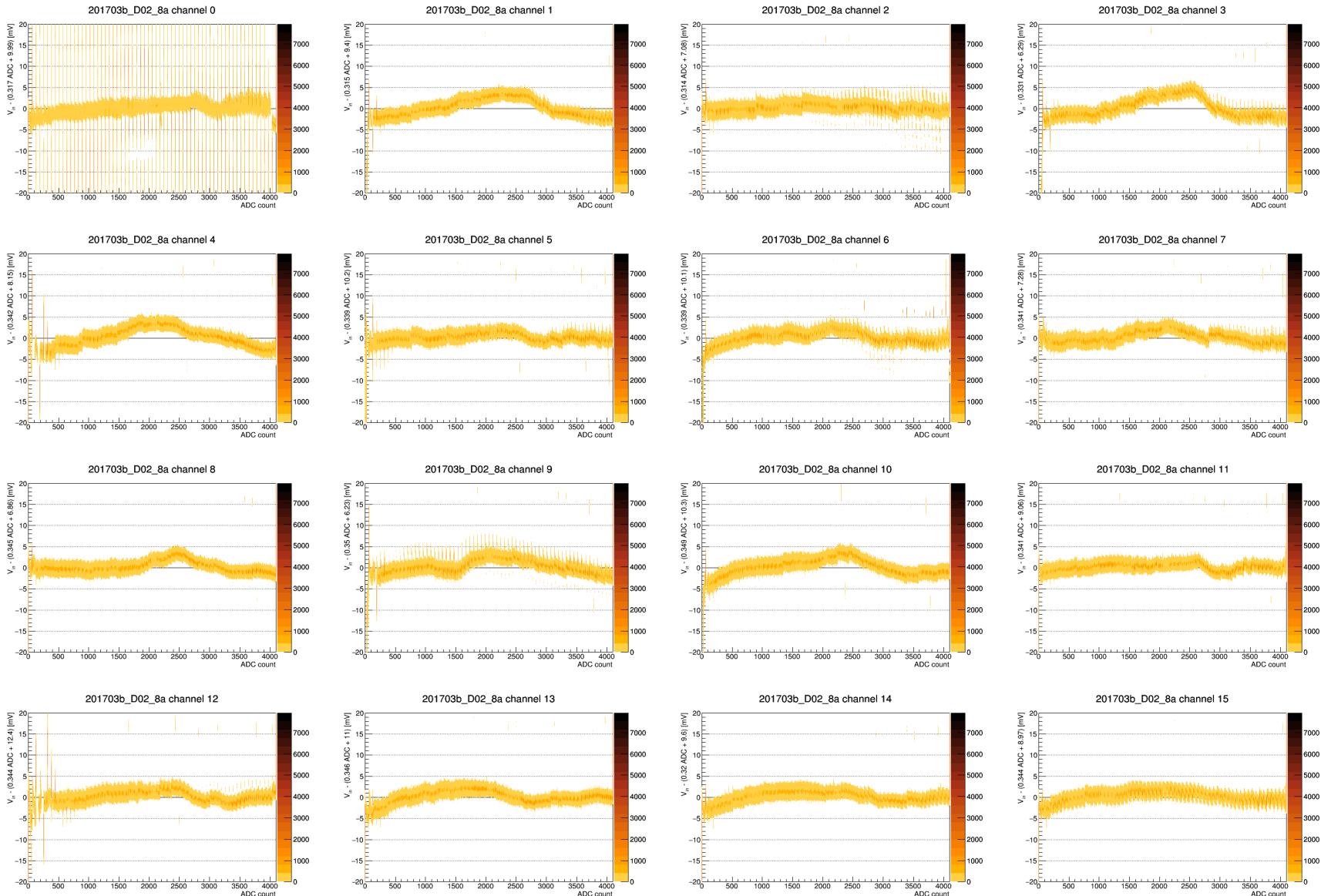
Residuals: chip D02, time 7a



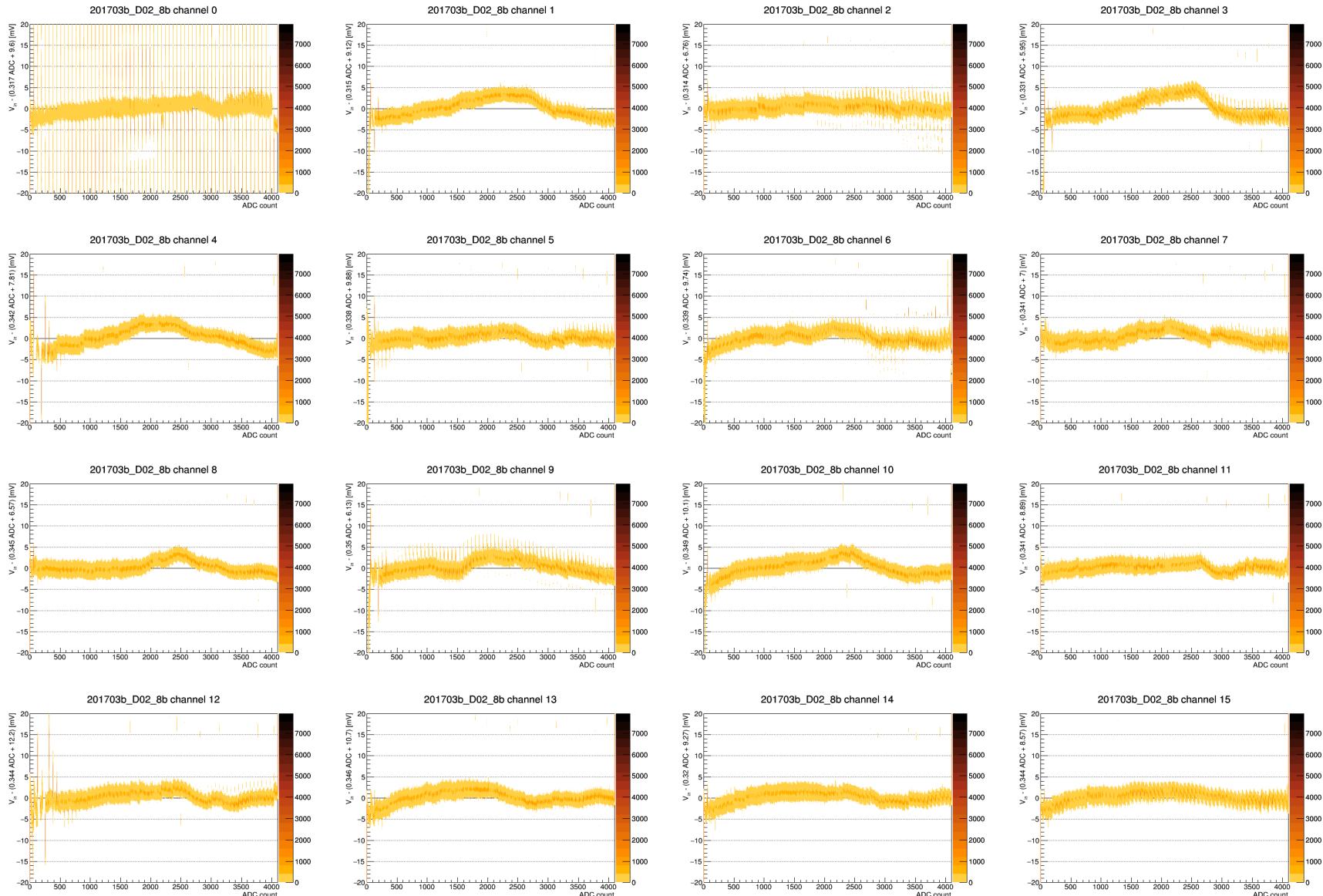
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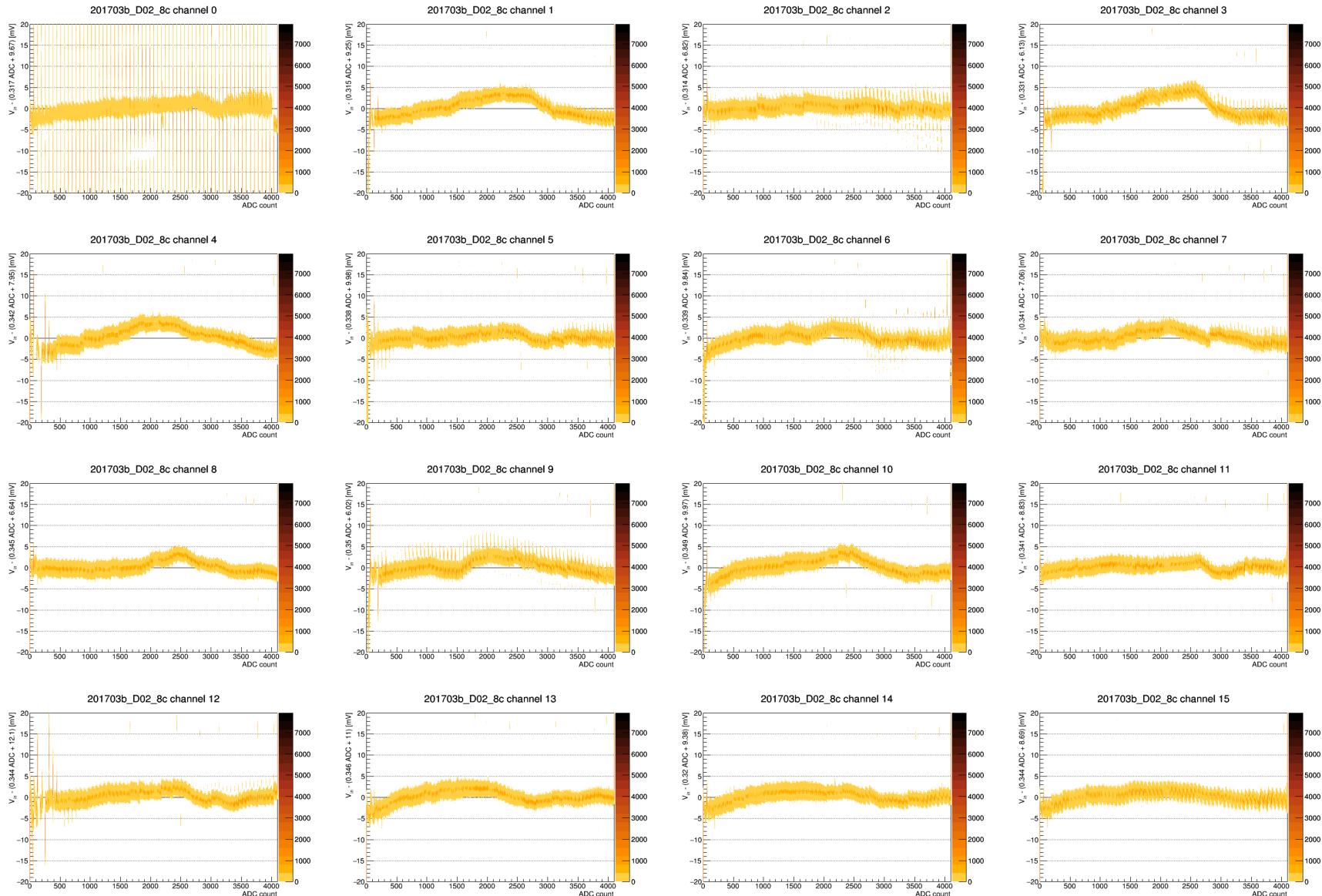
Residuals: chip D02, time 8a



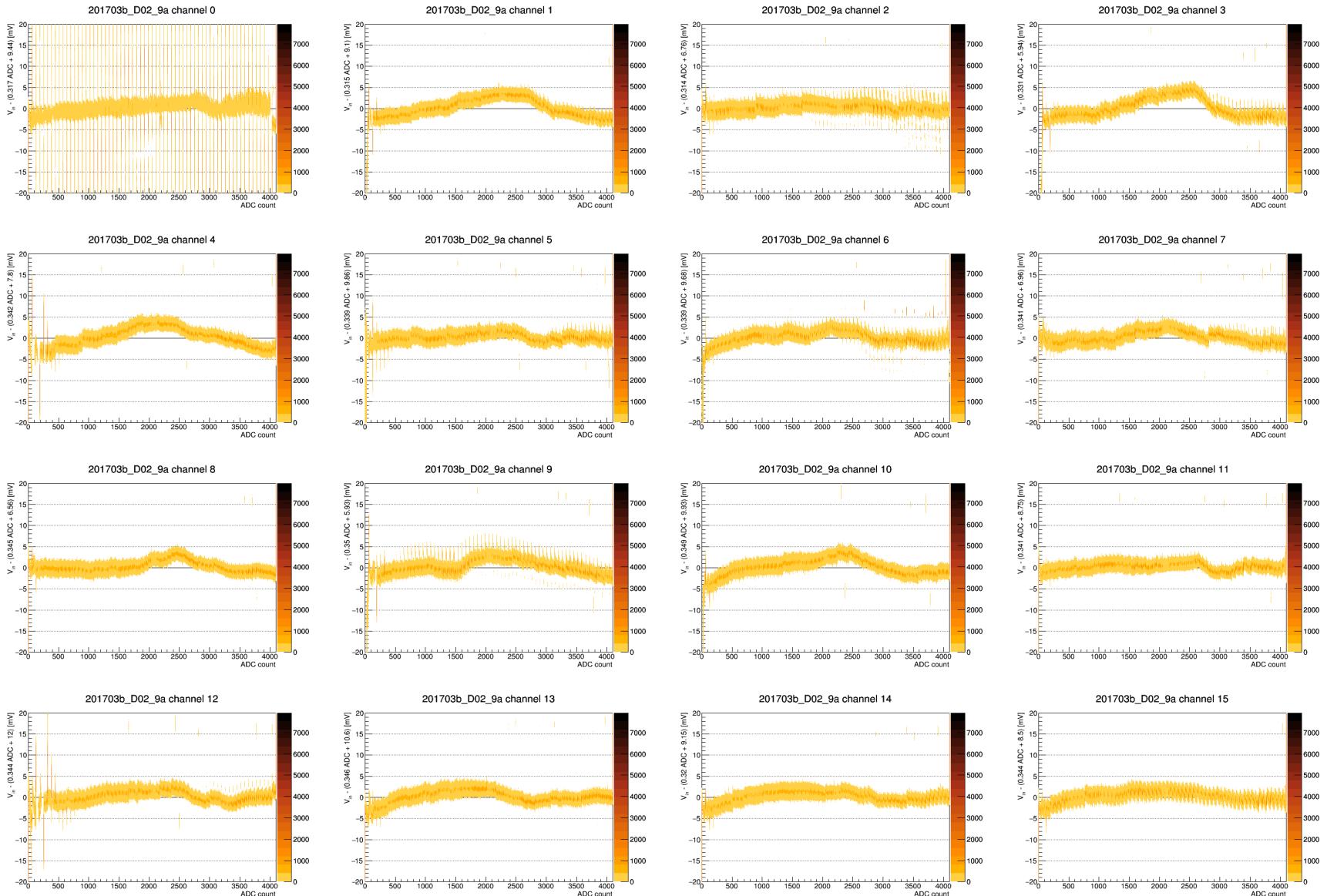
Residuals: chip D02, time 8b



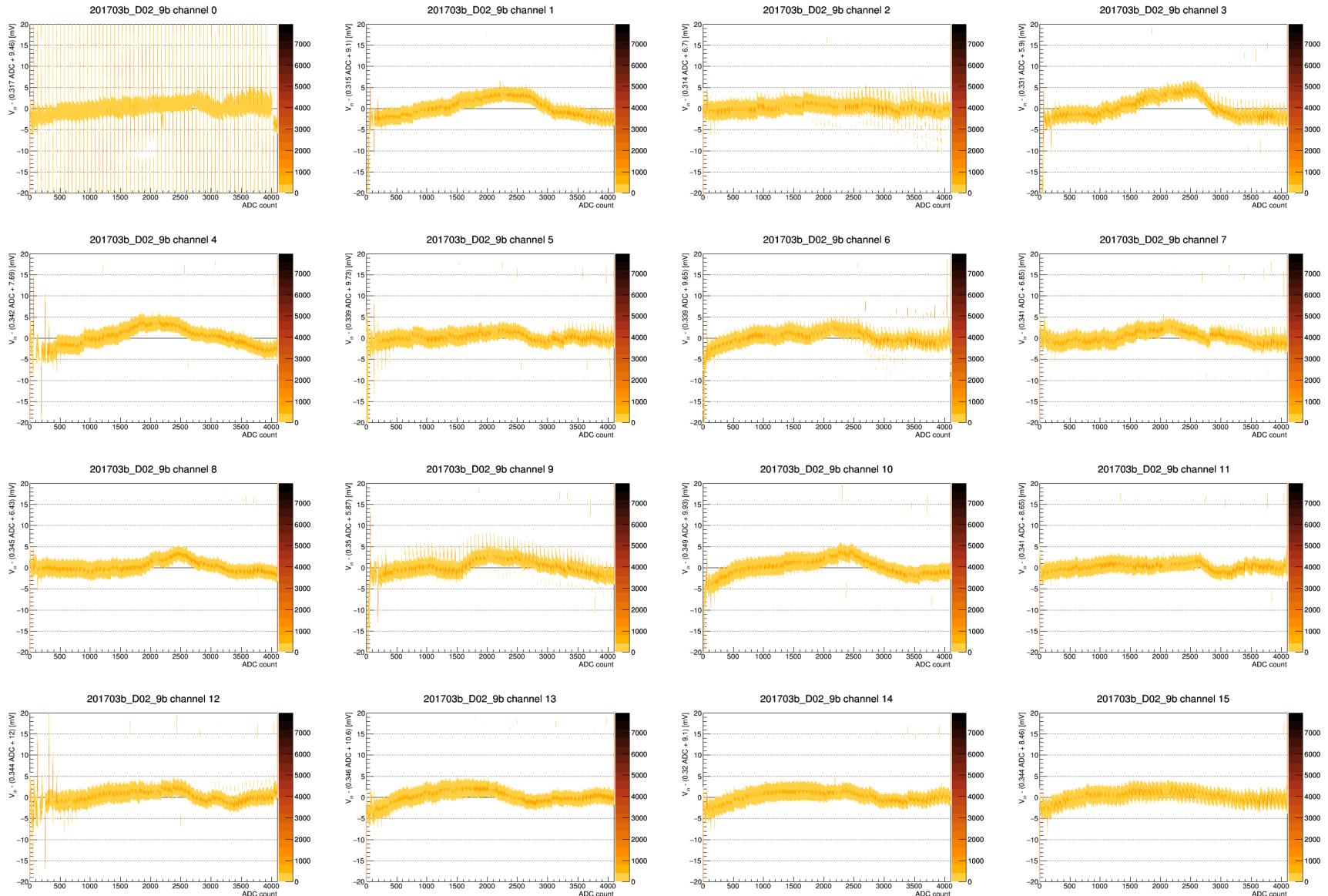
Residuals: chip D02, time 8c



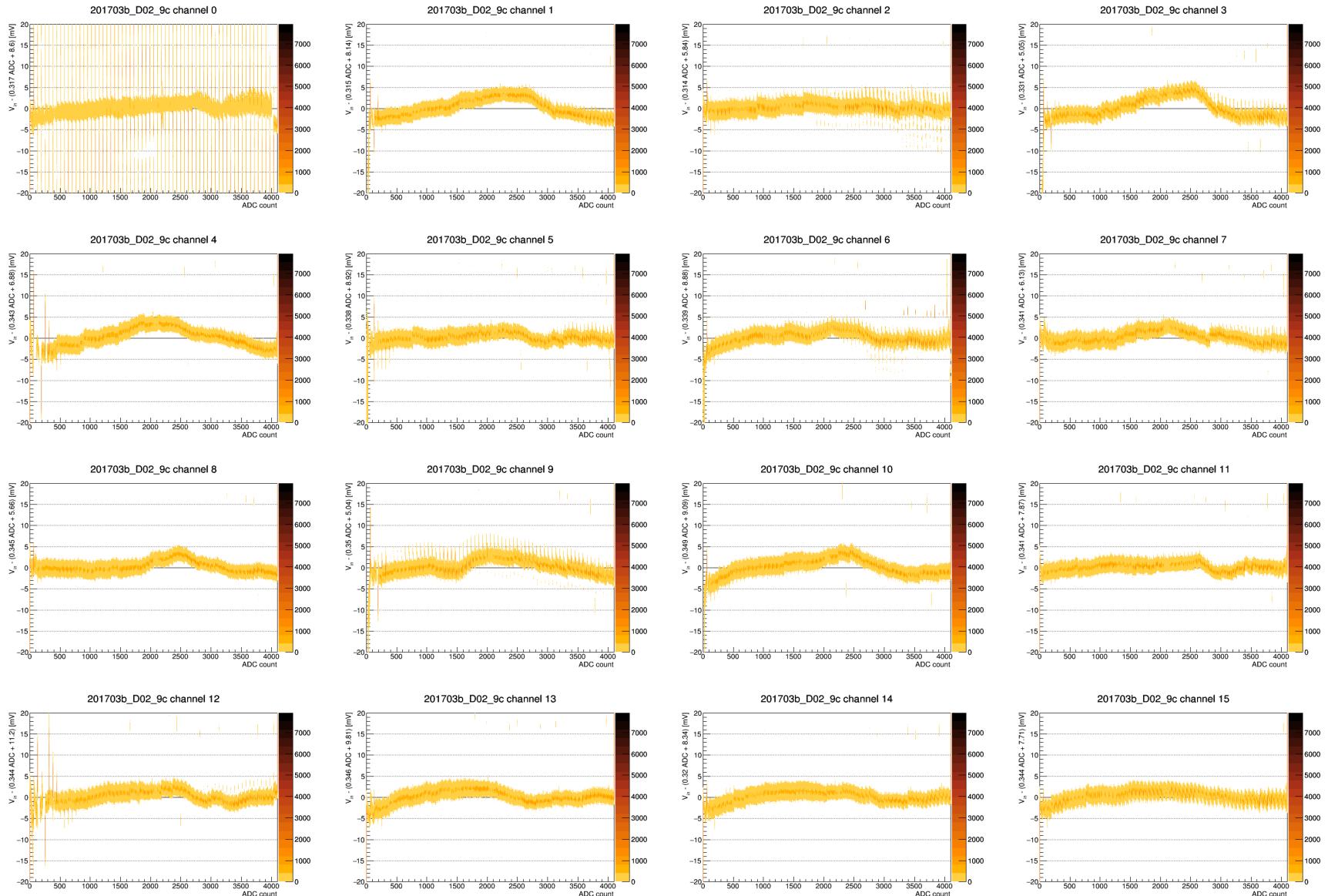
Residuals: chip D02, time 9a



Residuals: chip D02, time 9b

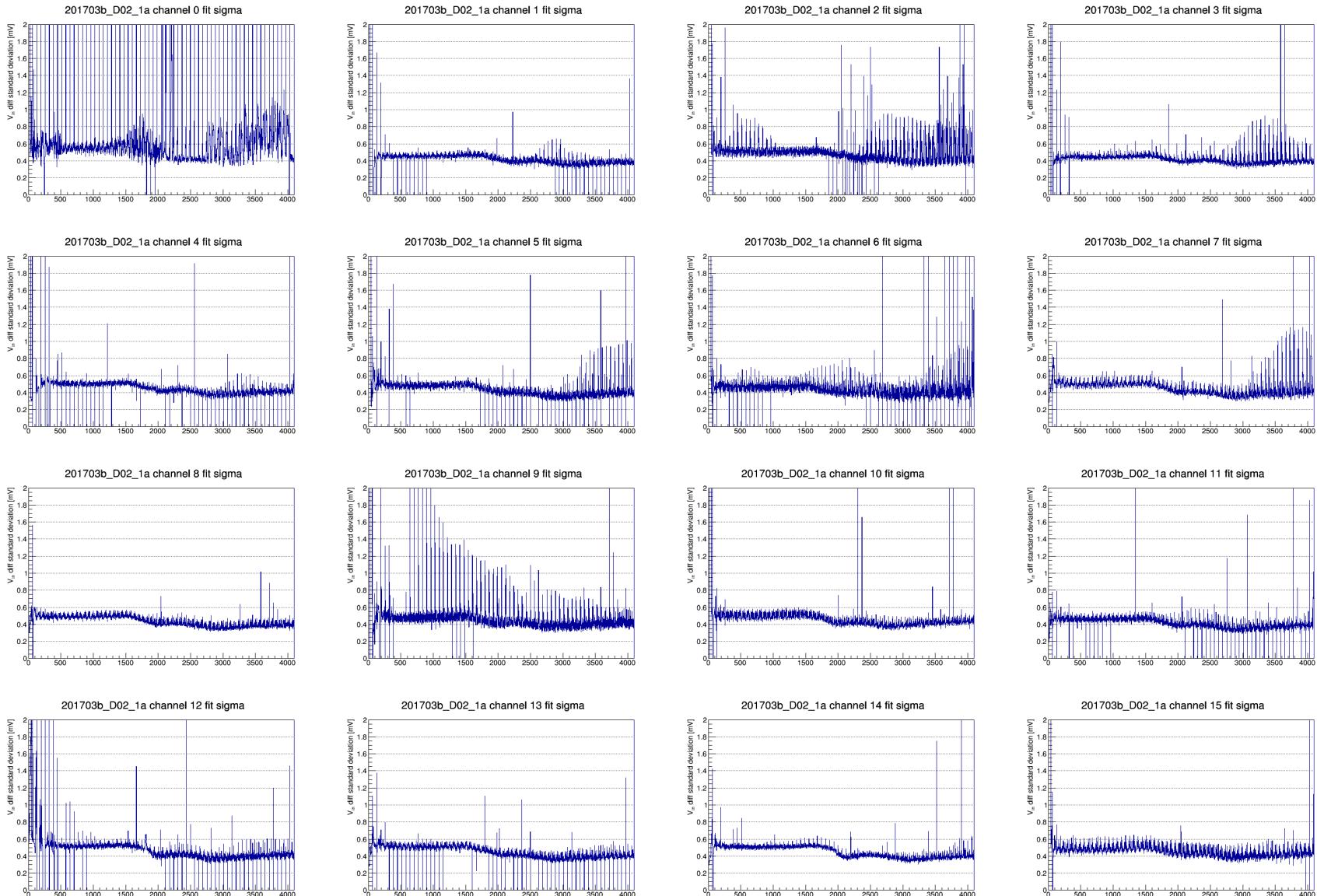


Residuals: chip D02, time 9c

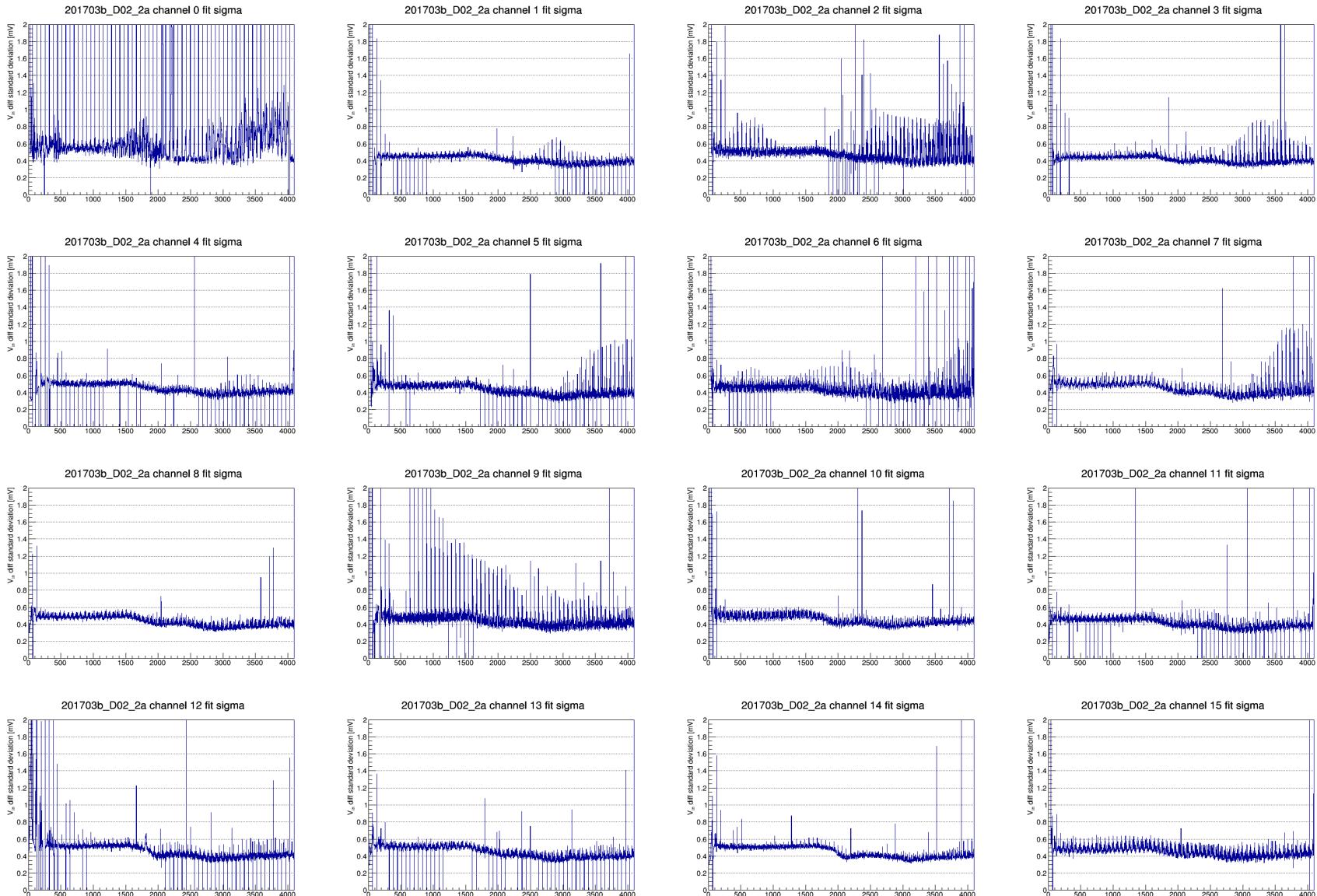


Bin RMS

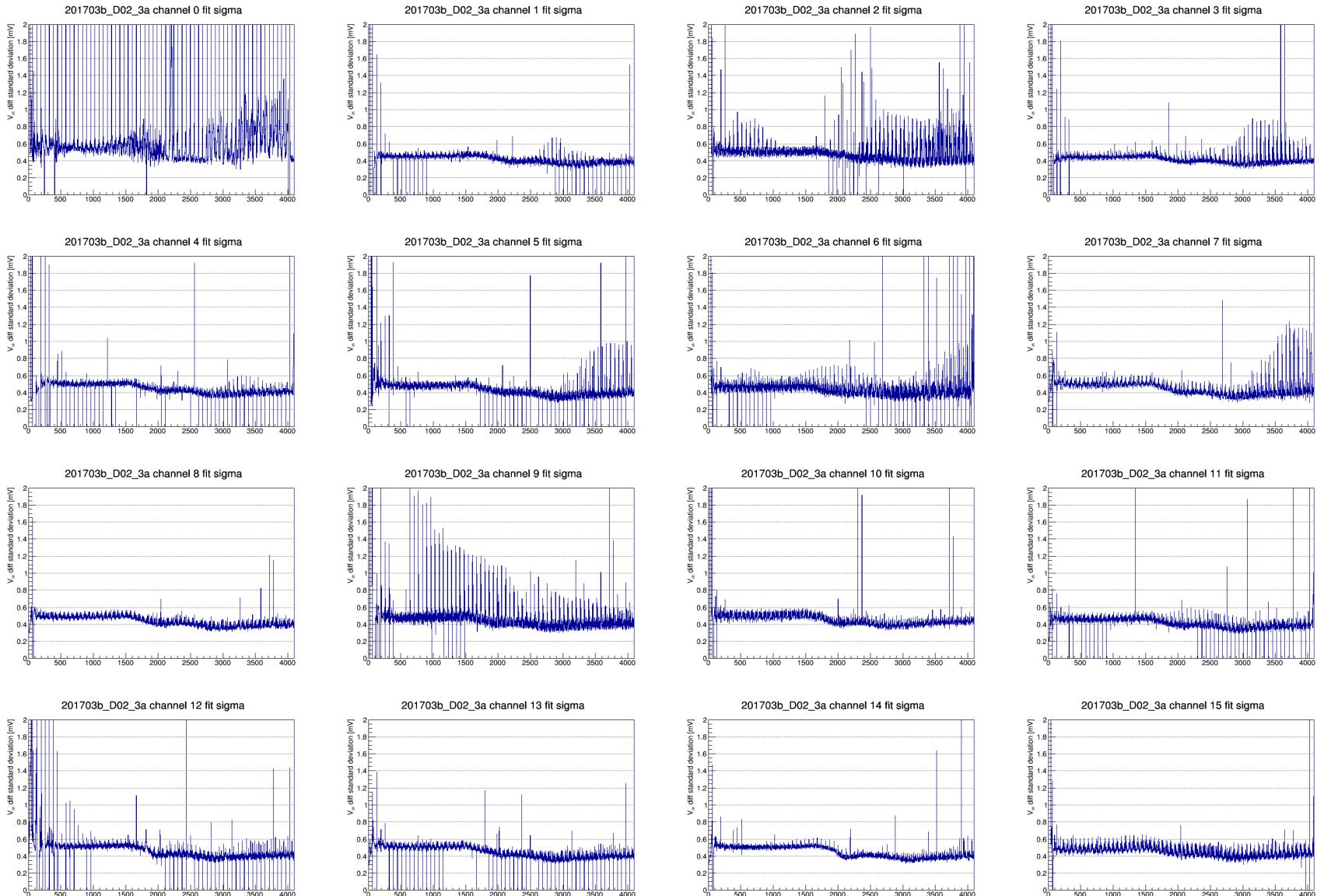
Bin RMS: chip D02, time 1a



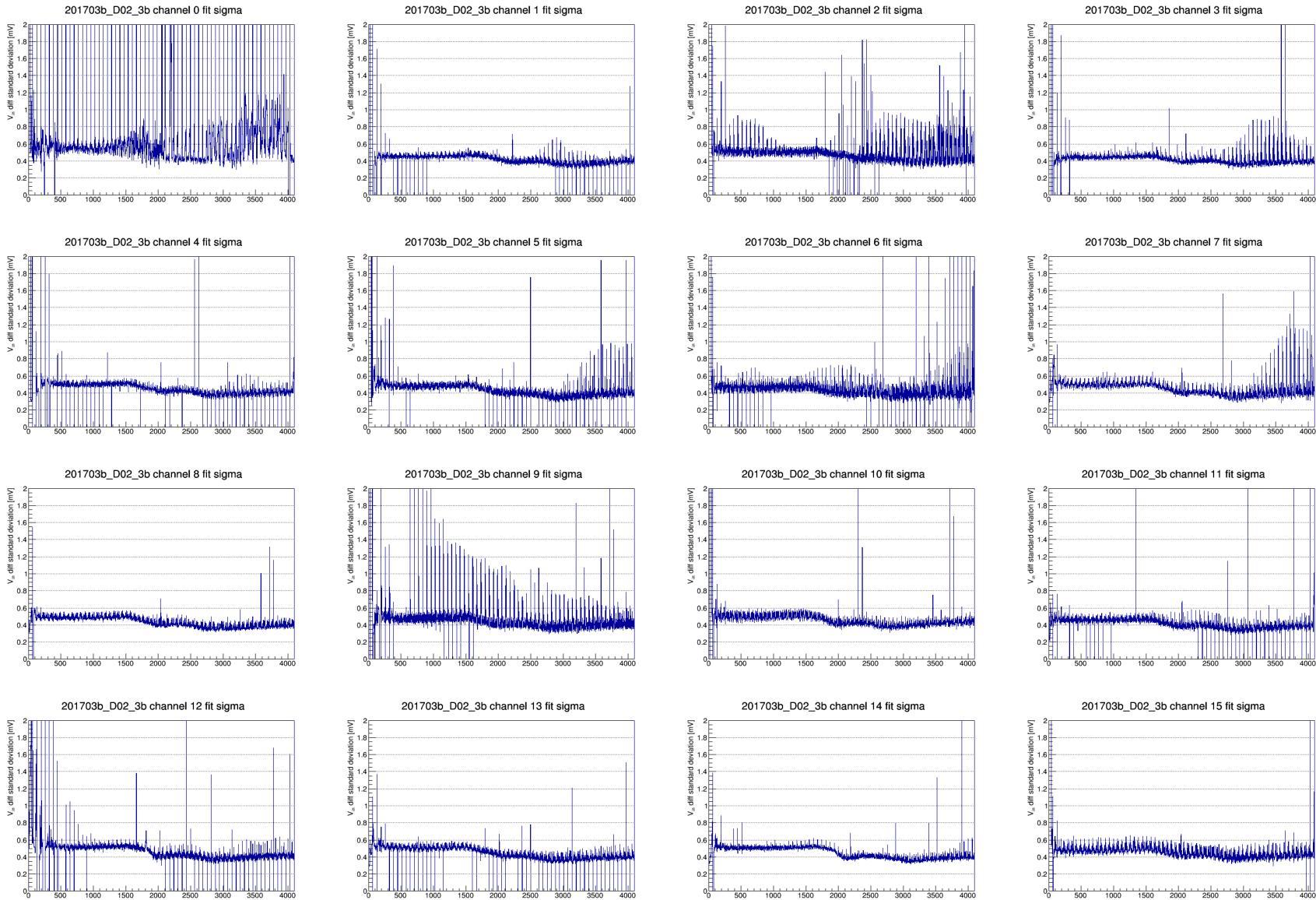
Bin RMS: chip D02, time 2a



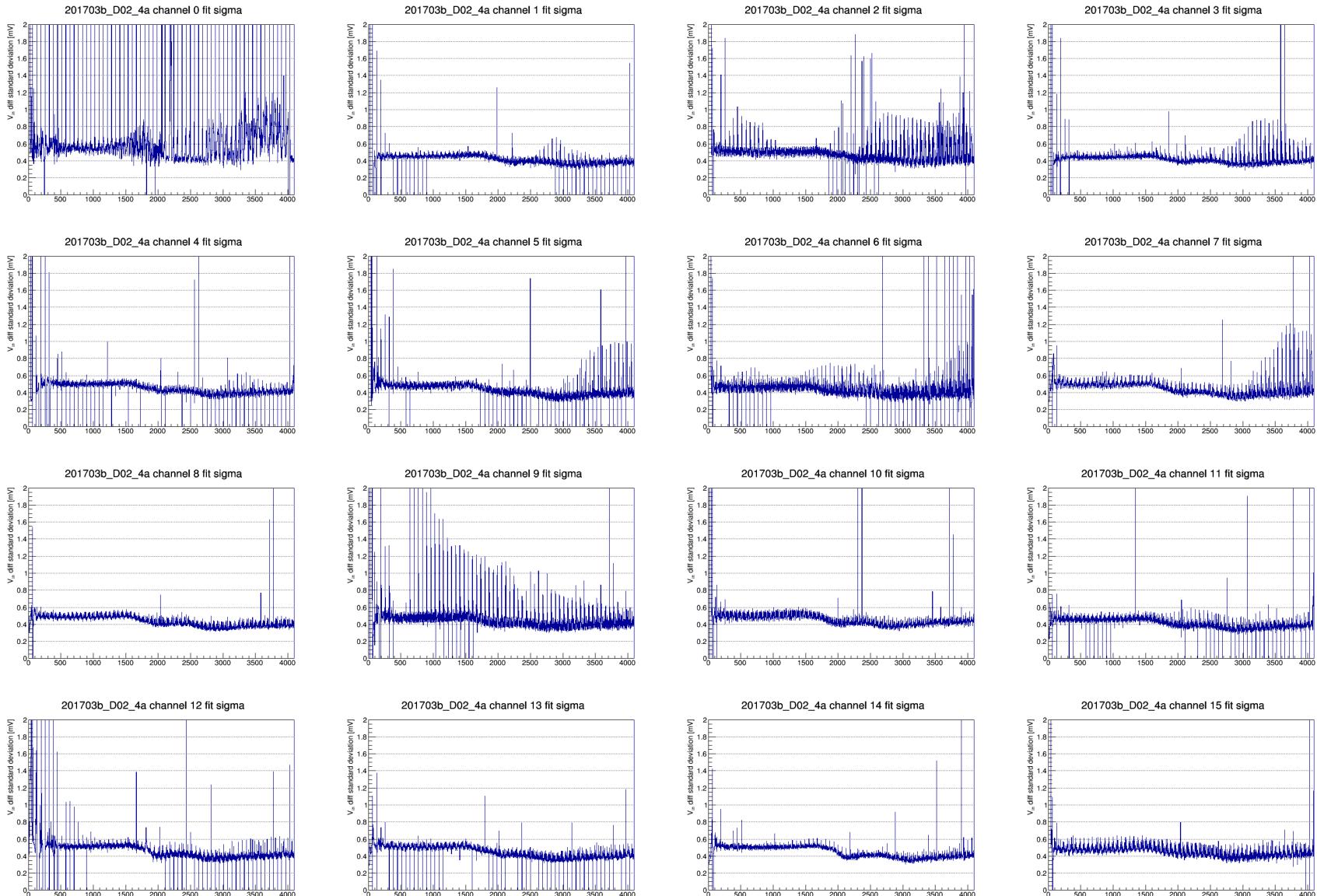
Bin RMS: chip D02, time 3a



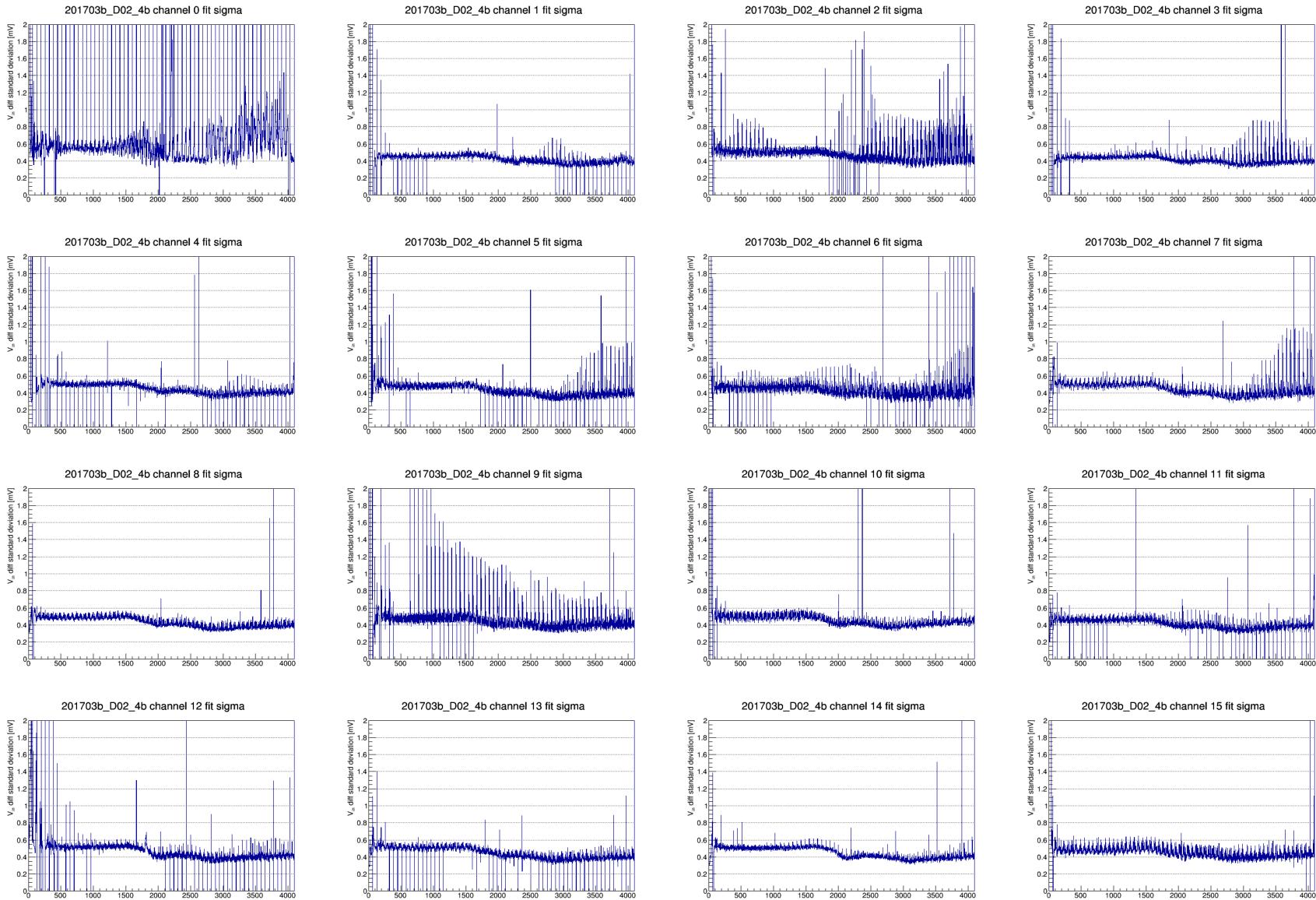
Bin RMS: chip D02, time 3b



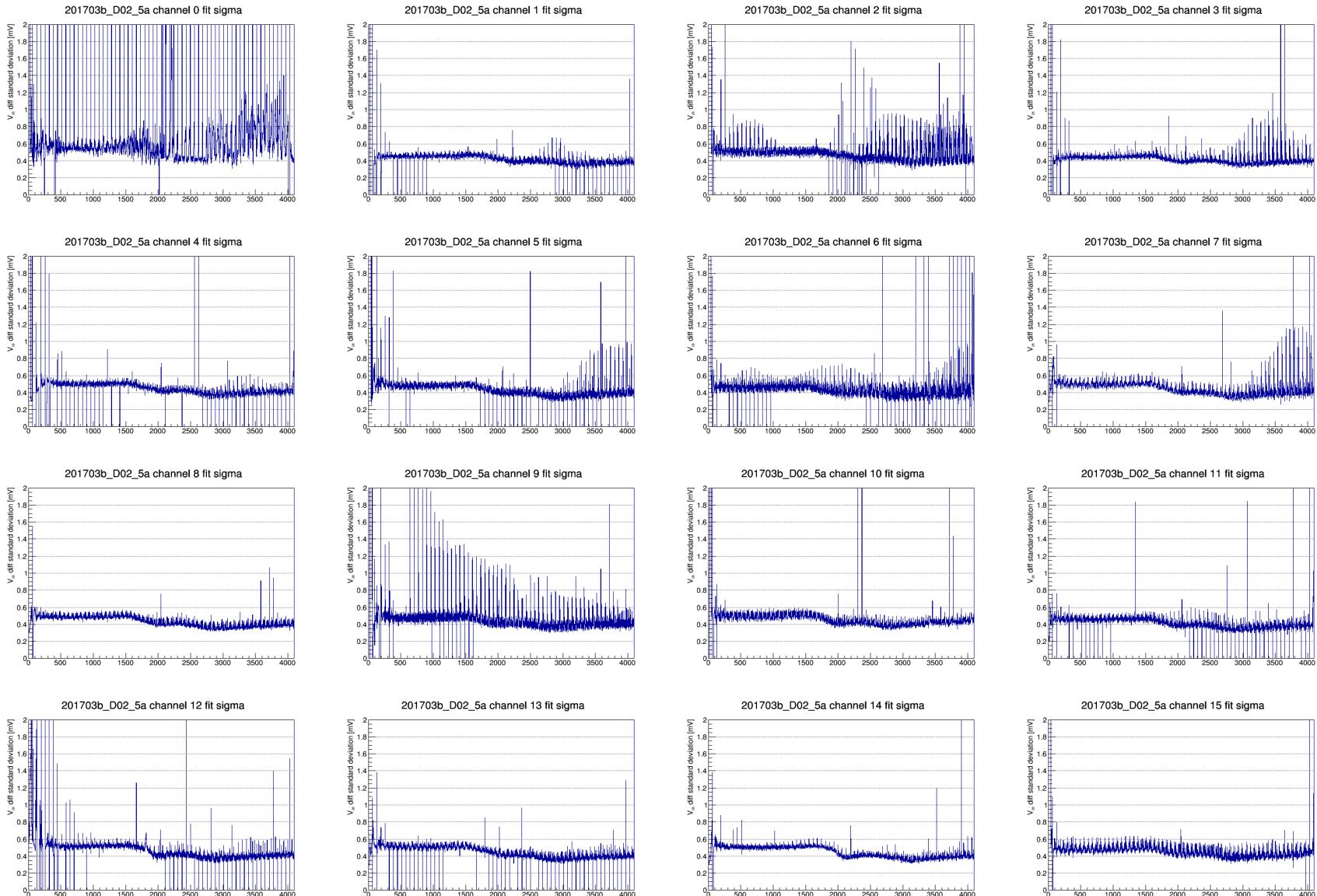
Bin RMS: chip D02, time 4a



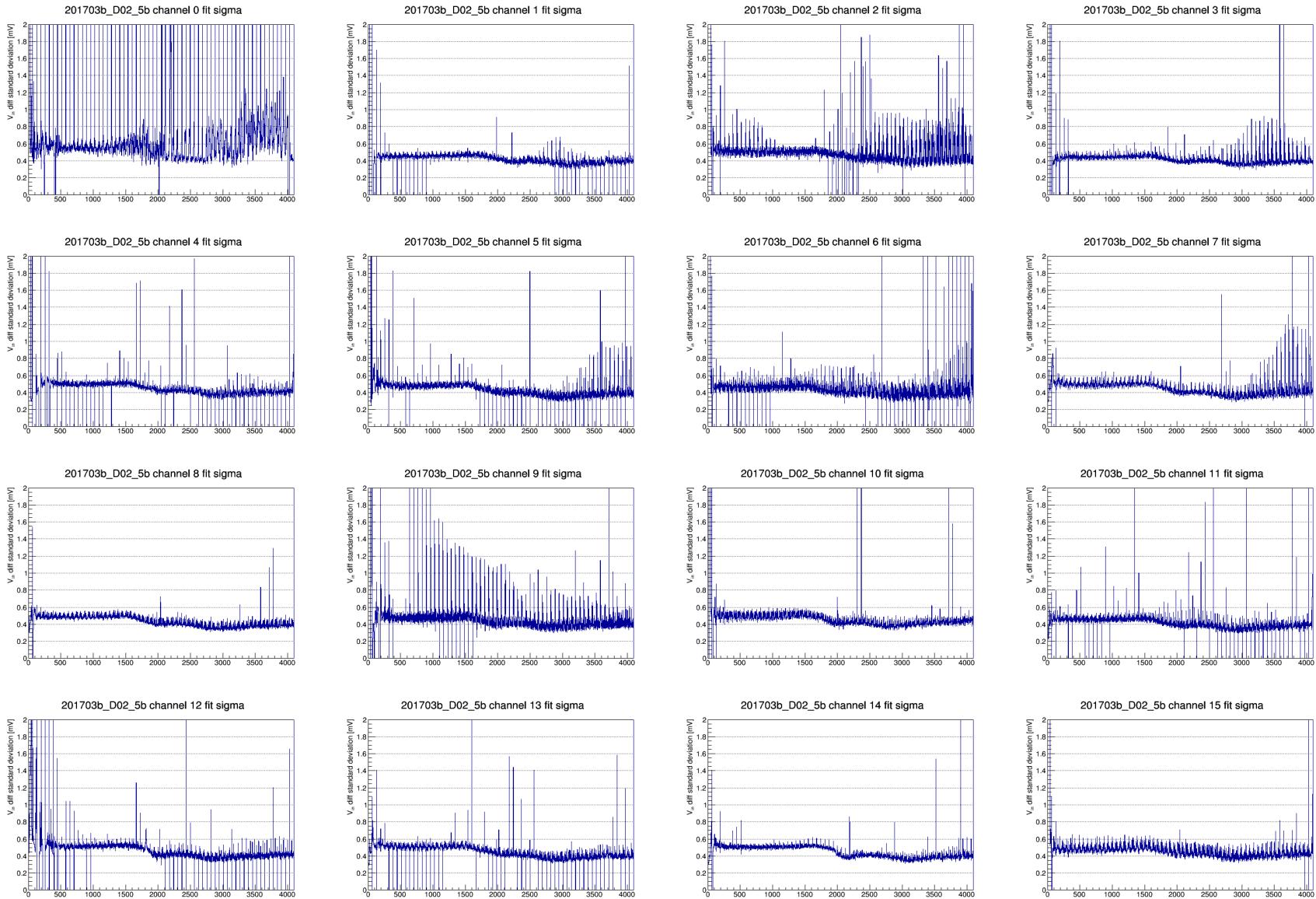
Bin RMS: chip D02, time 4b



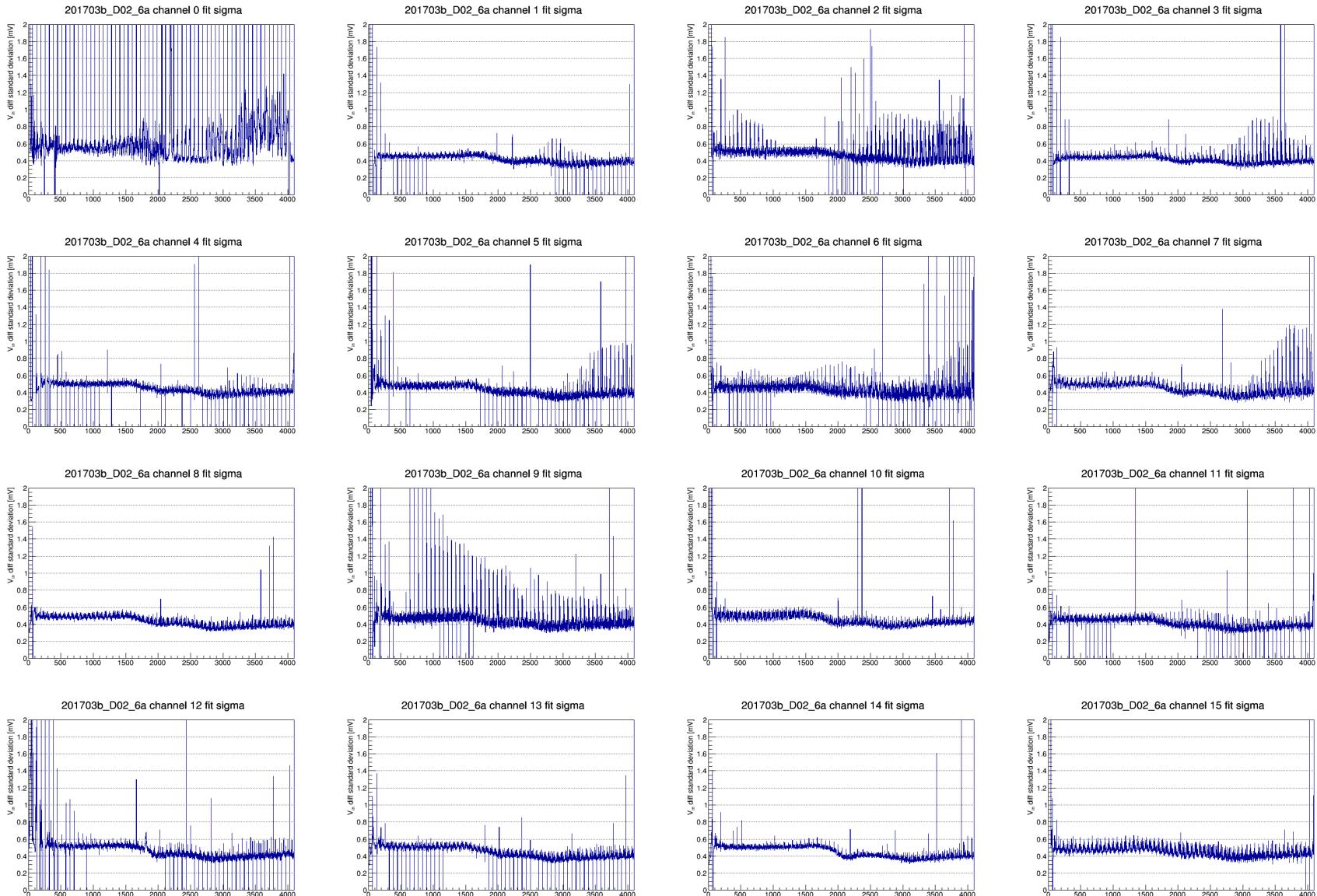
Bin RMS: chip D02, time 5a



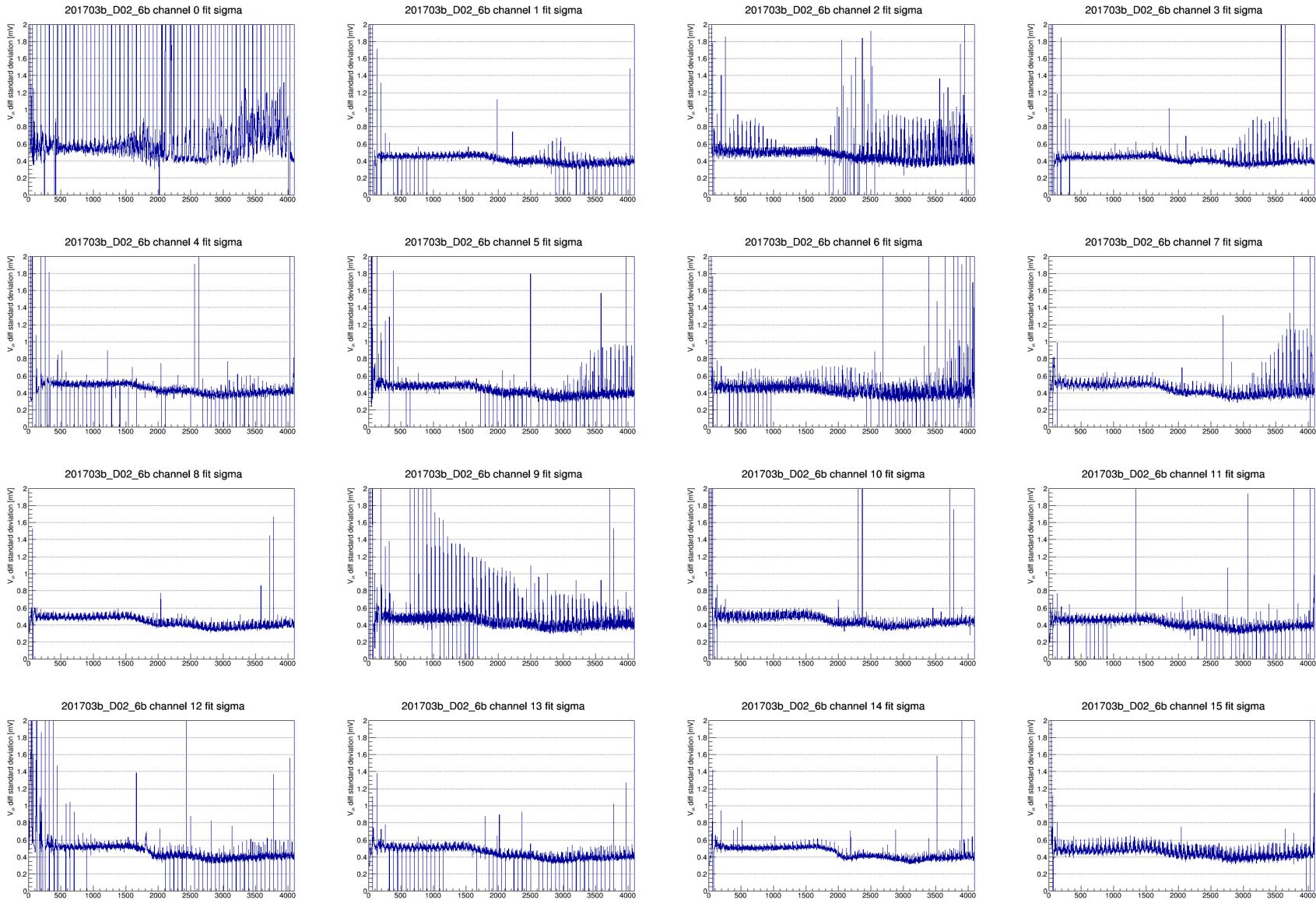
Bin RMS: chip D02, time 5b



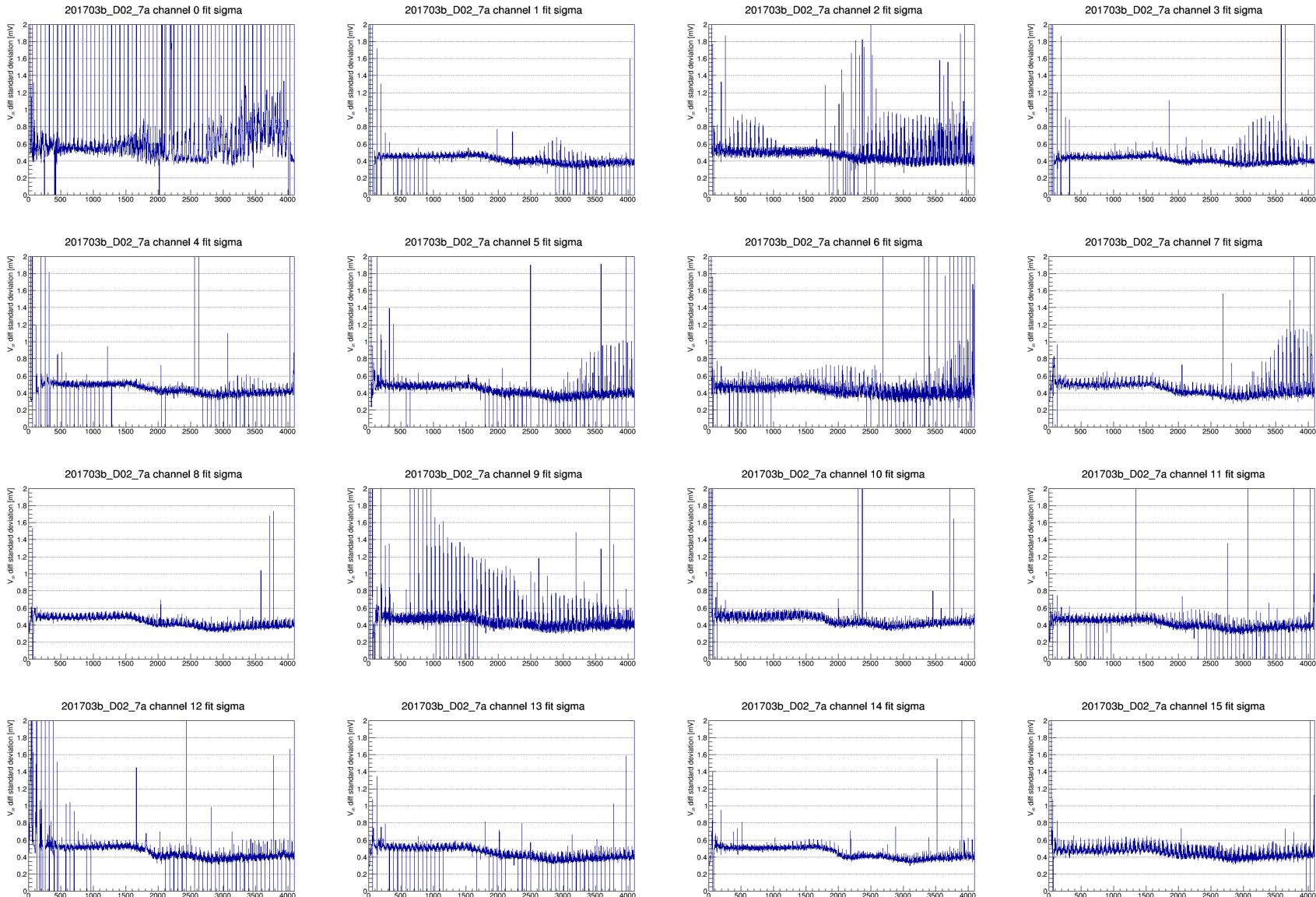
Bin RMS: chip D02, time 6a



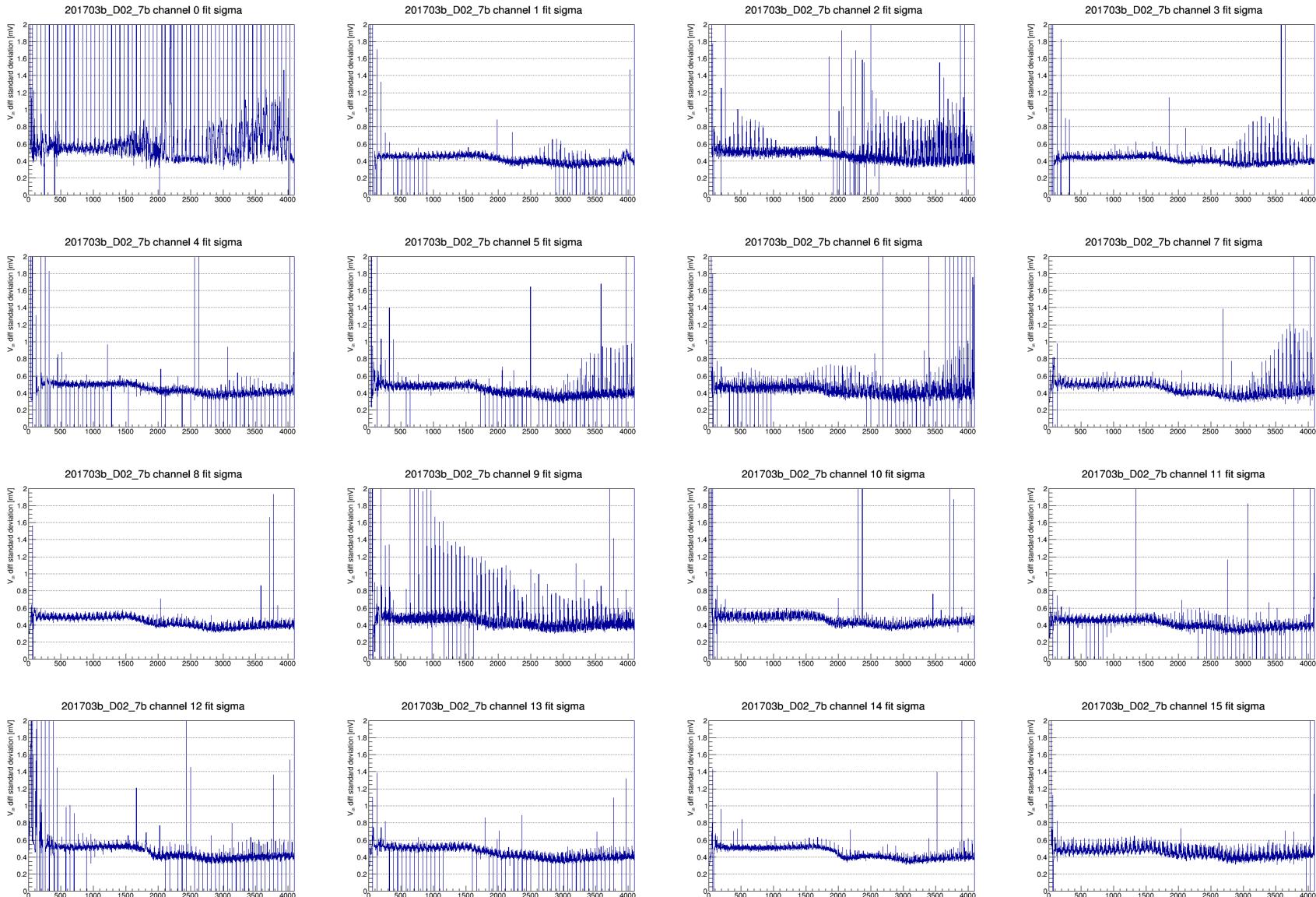
Bin RMS: chip D02, time 6b



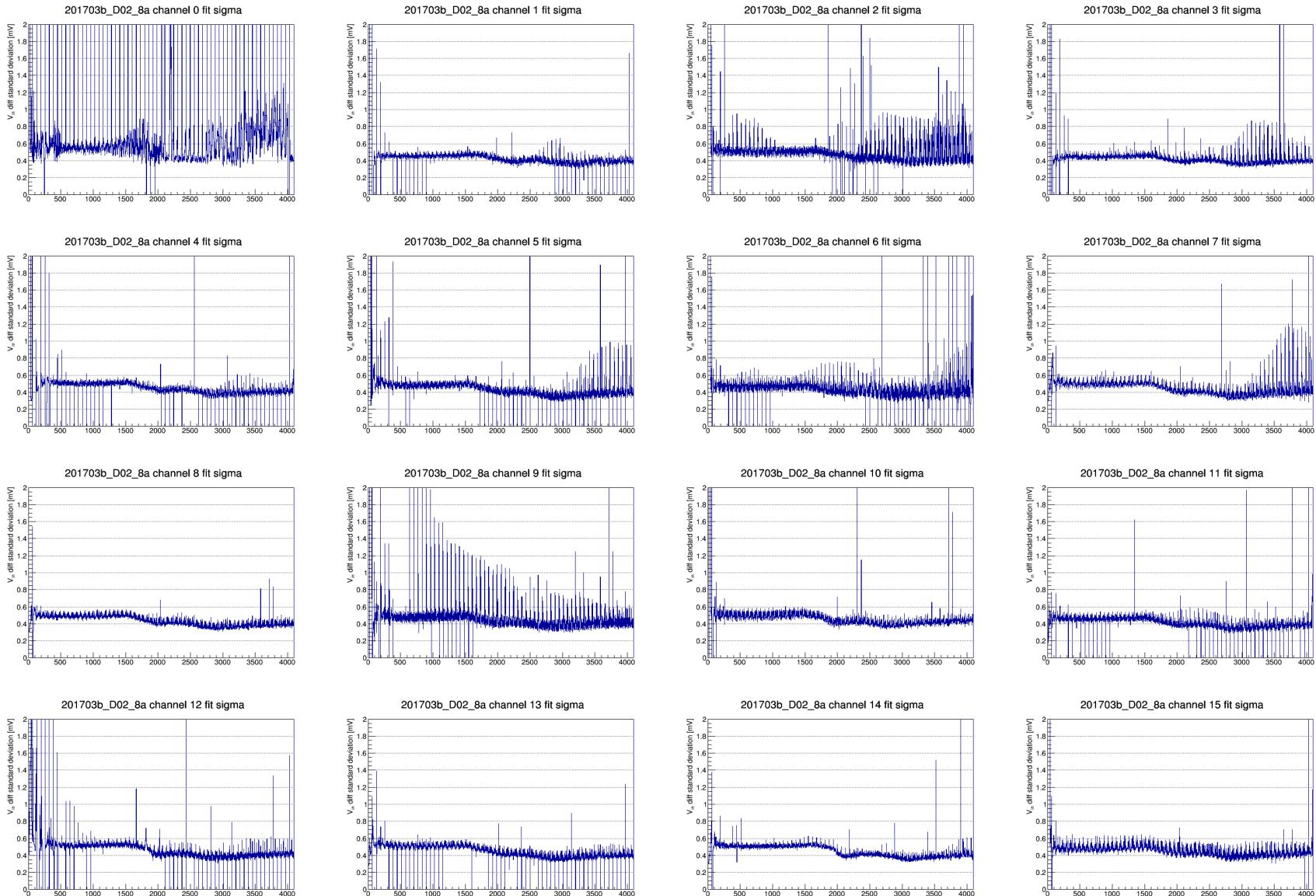
Bin RMS: chip D02, time 7a



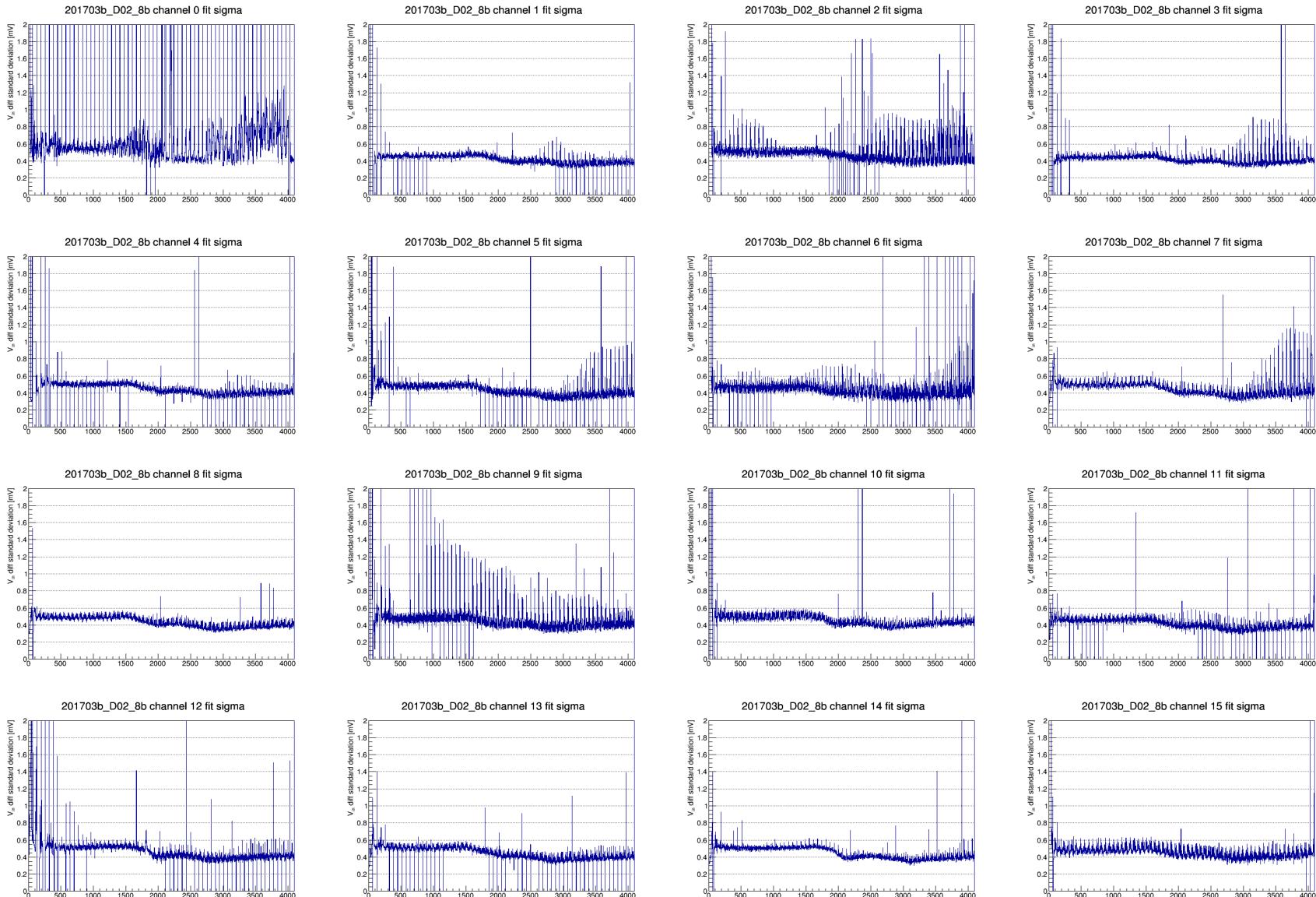
Bin RMS: chip D02, time 7b



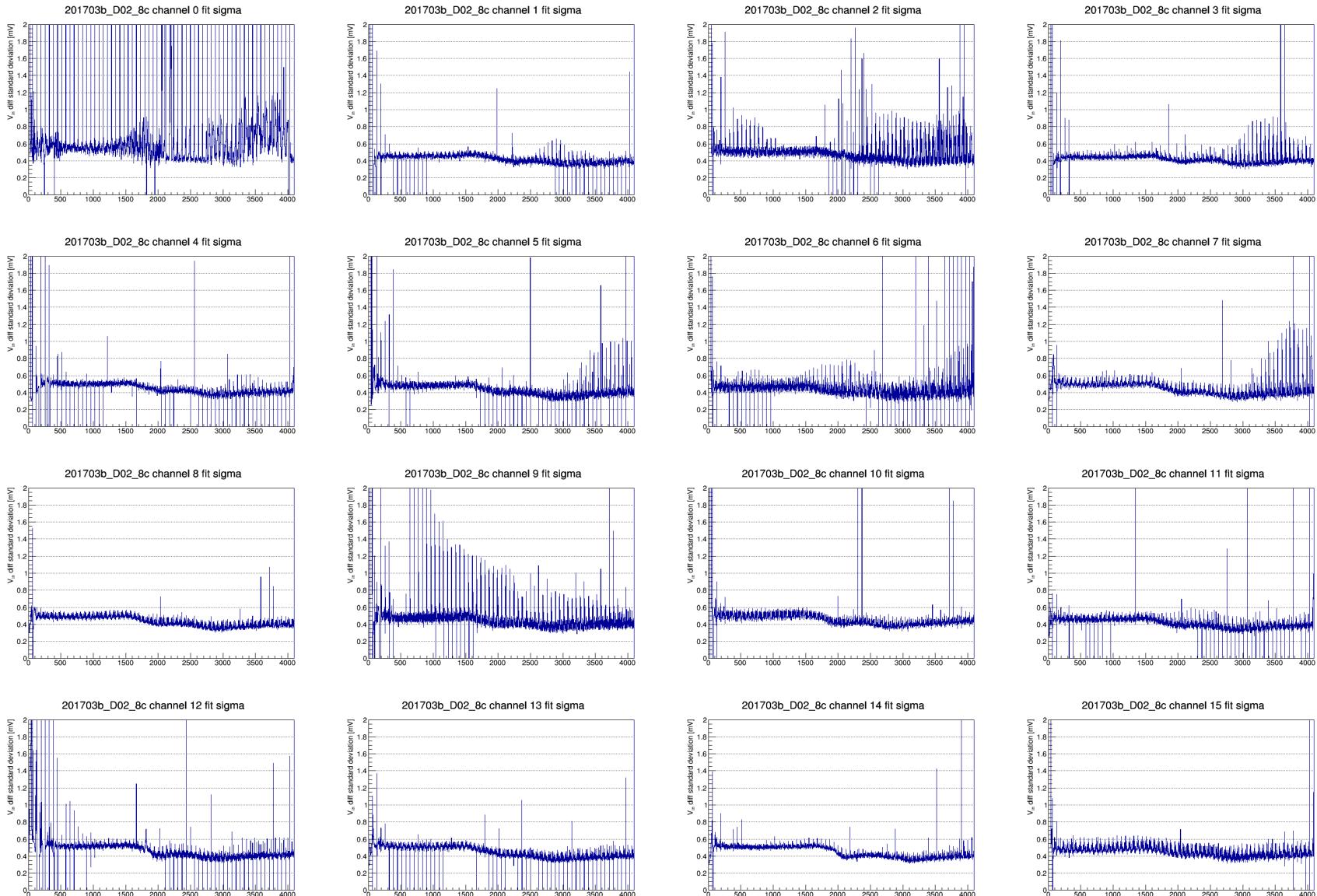
Bin RMS: chip D02, time 8a



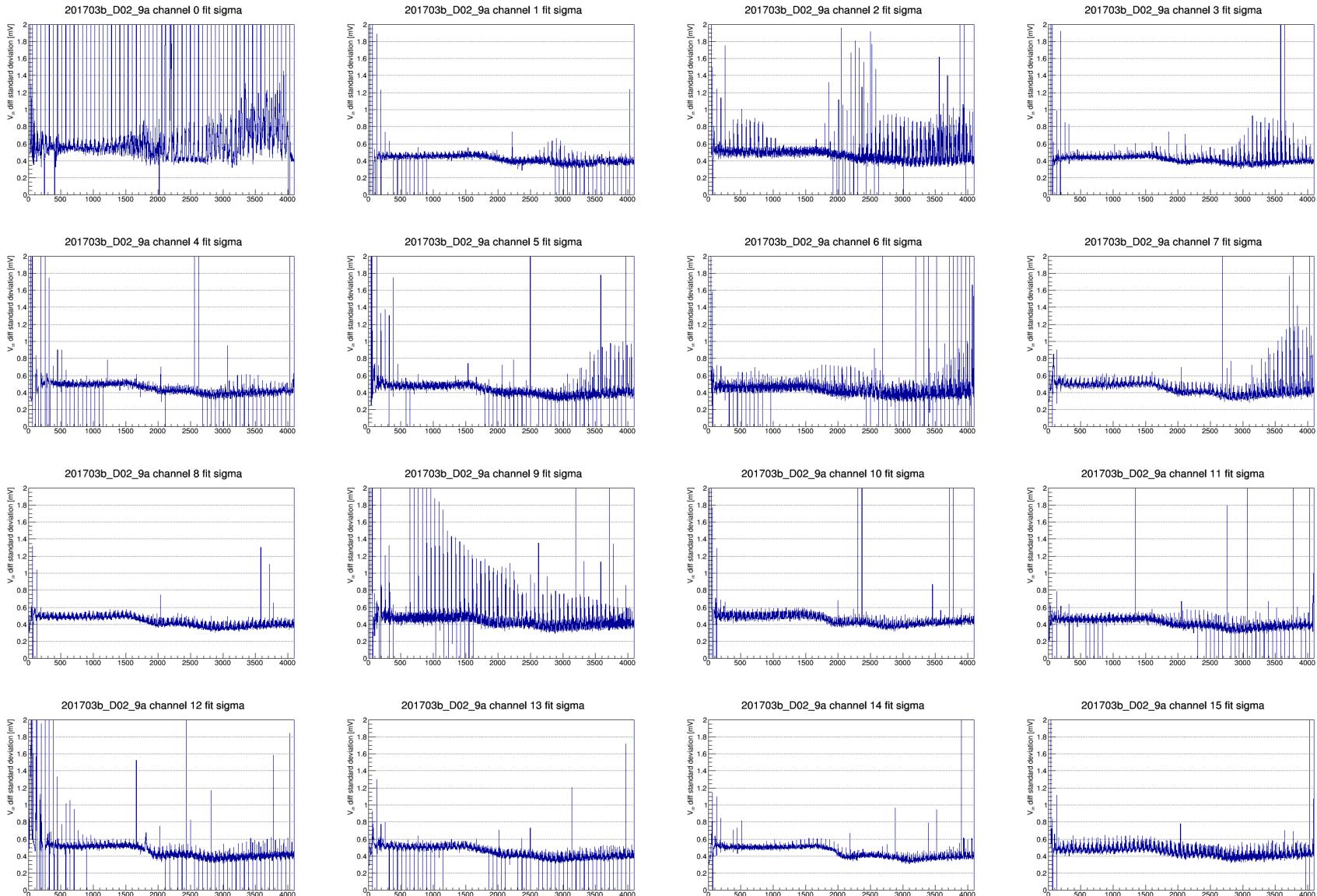
Bin RMS: chip D02, time 8b



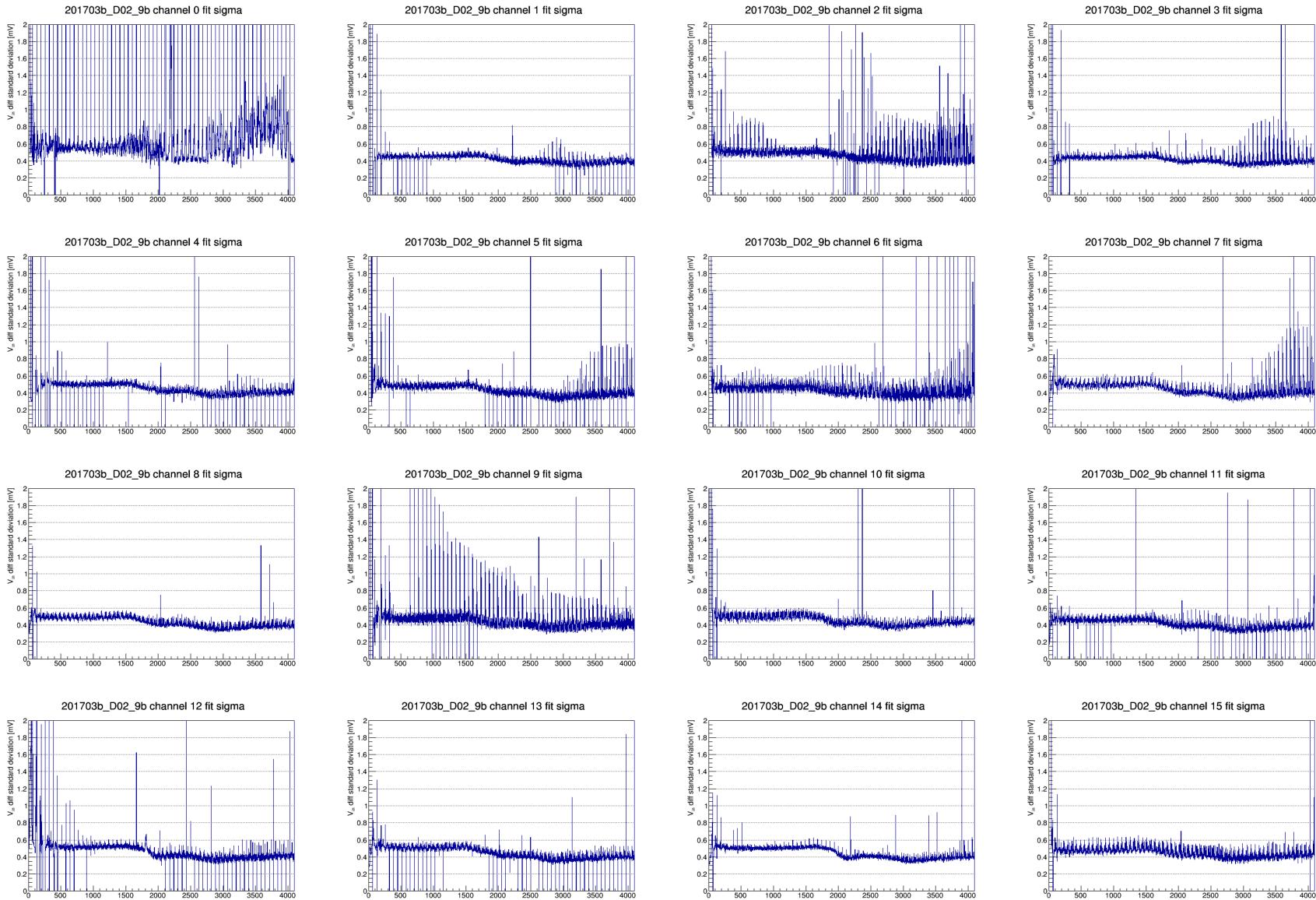
Bin RMS: chip D02, time 8c



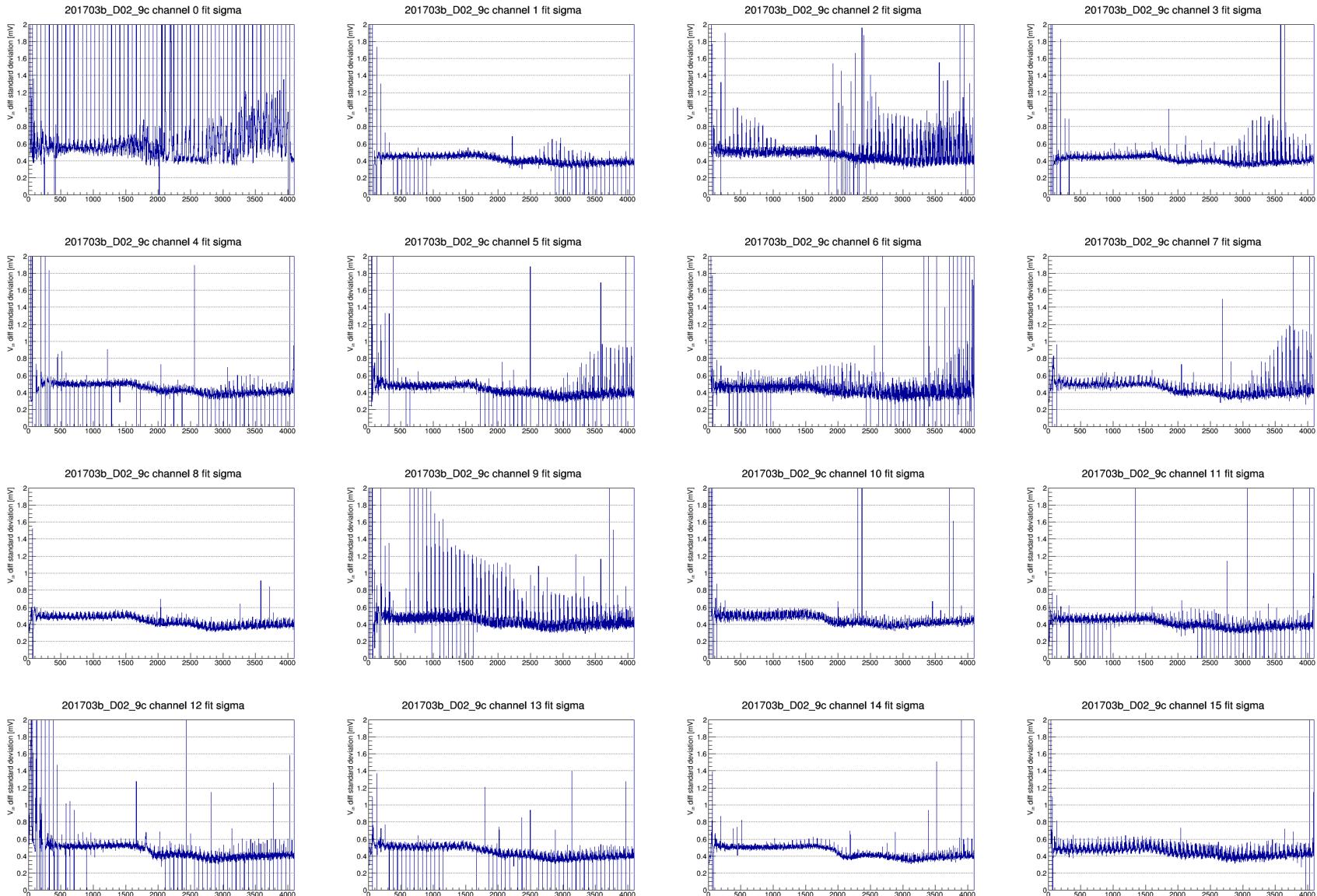
Bin RMS: chip D02, time 9a



Bin RMS: chip D02, time 9b

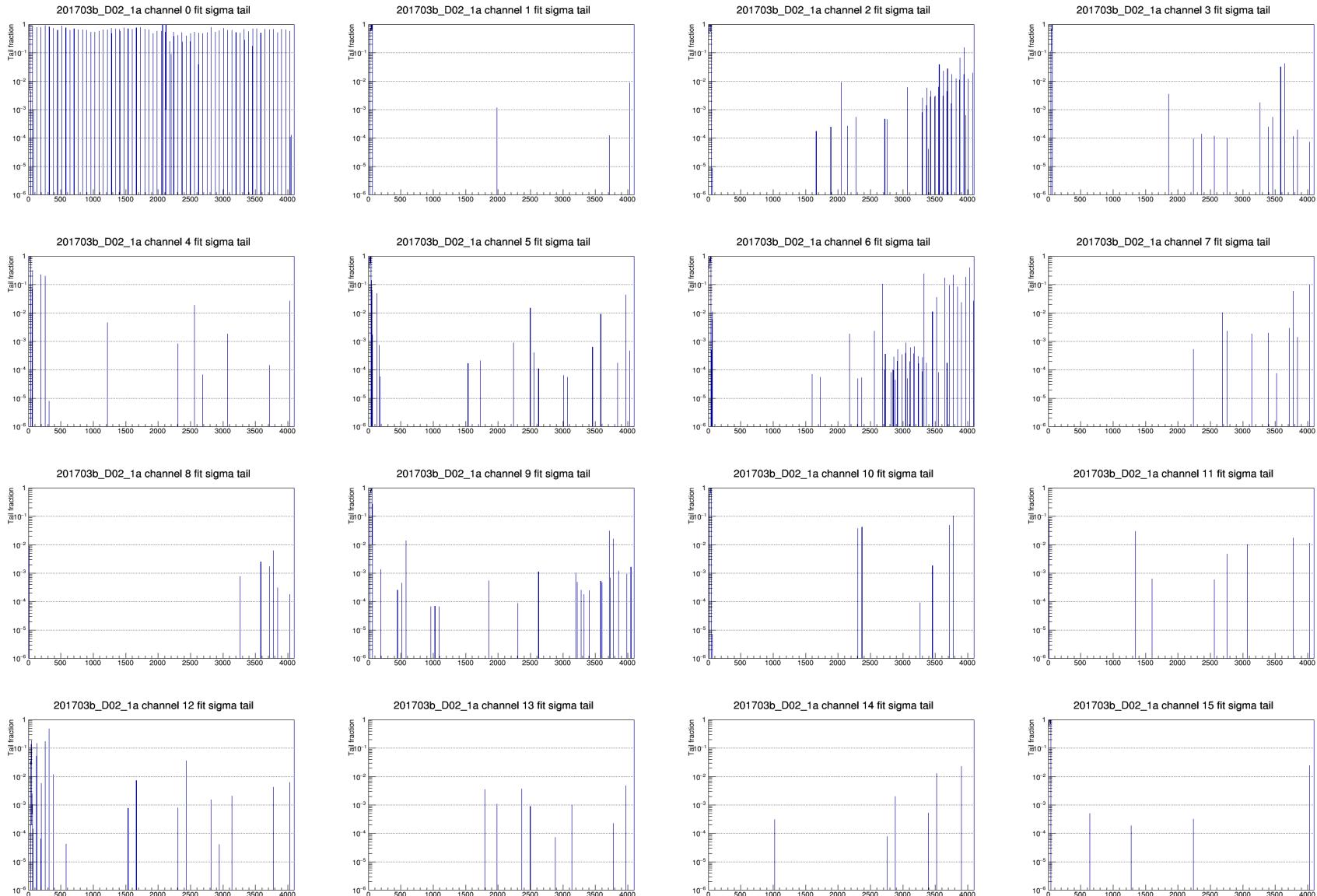


Bin RMS: chip D02, time 9c

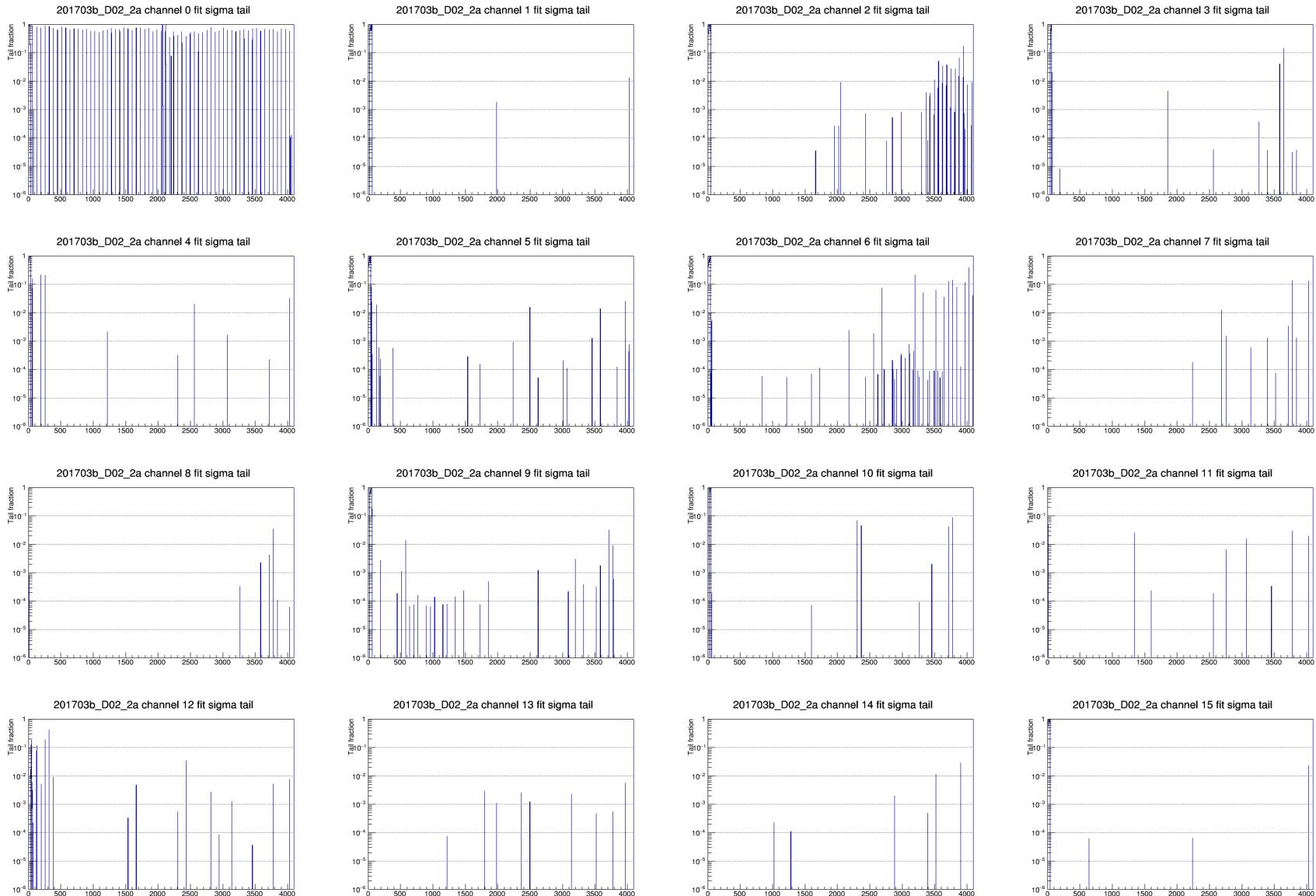


Tails

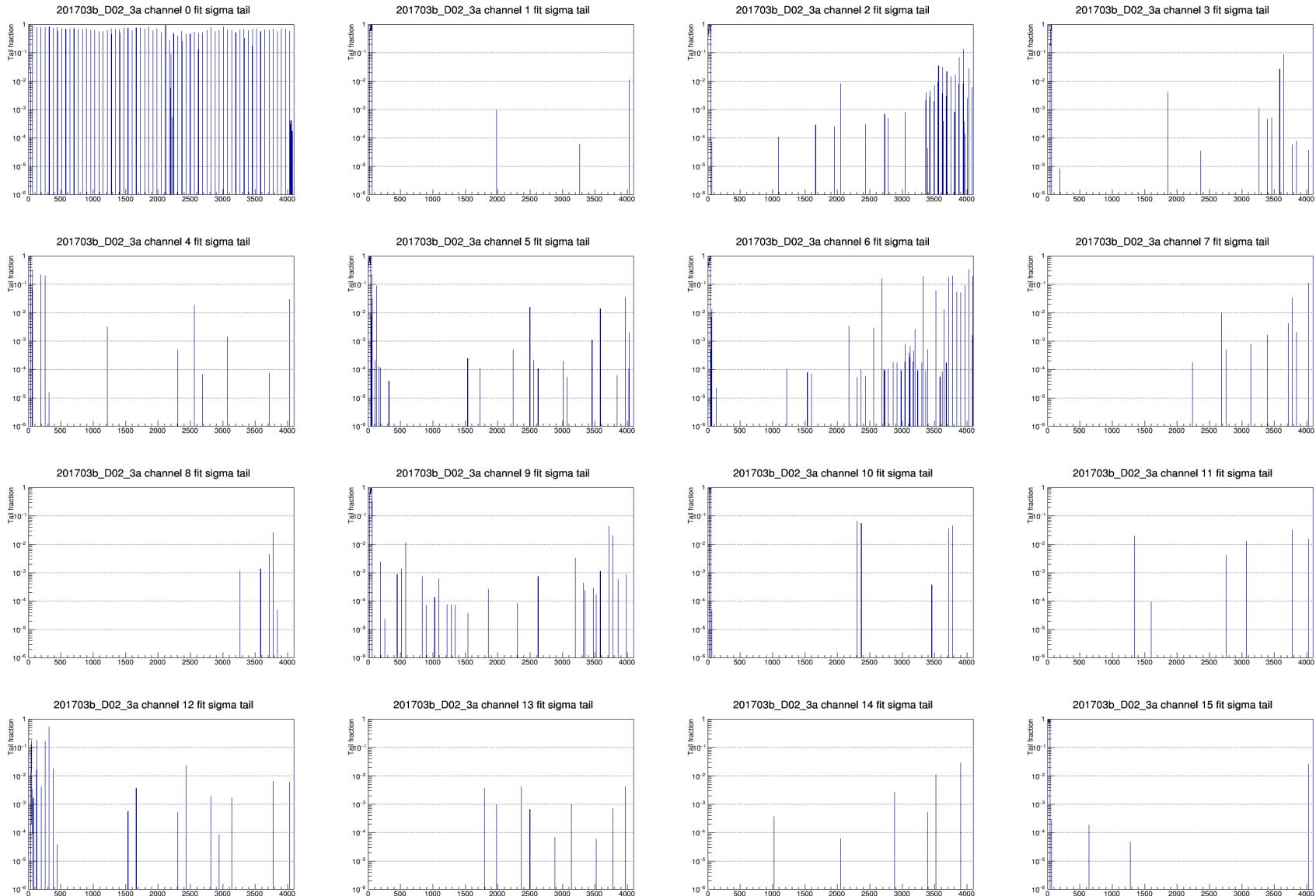
Tails: chip D02, time 1a



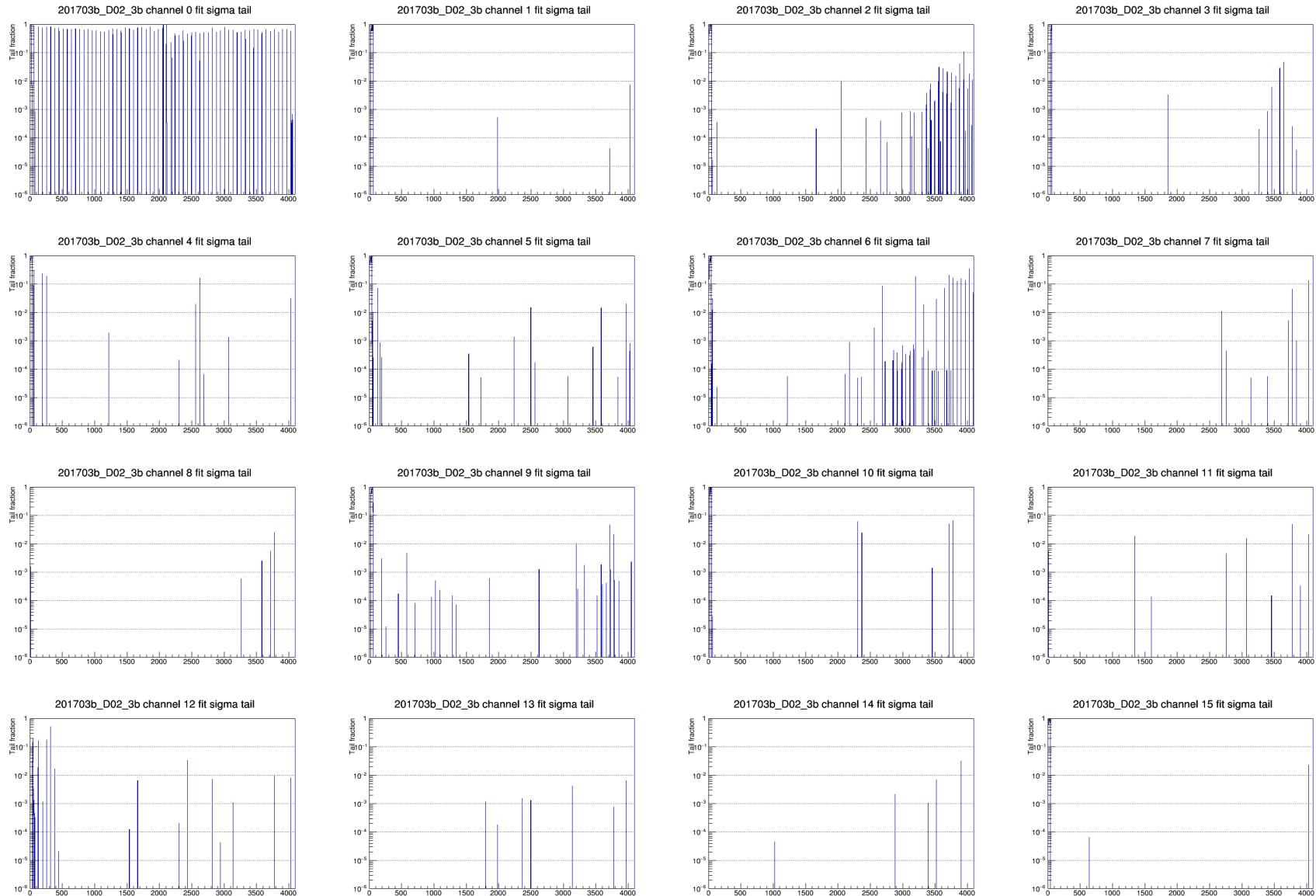
Tails: chip D02, time 2a



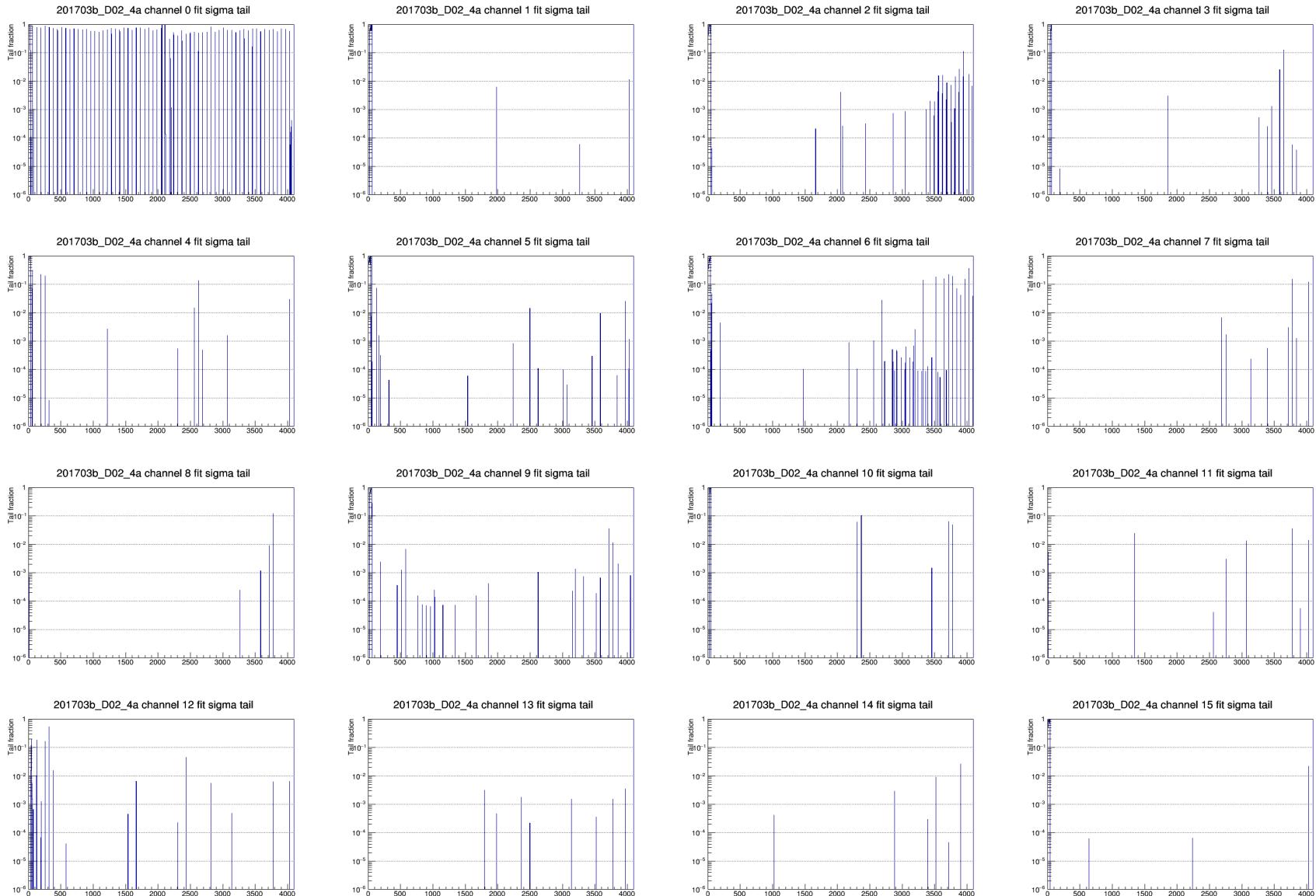
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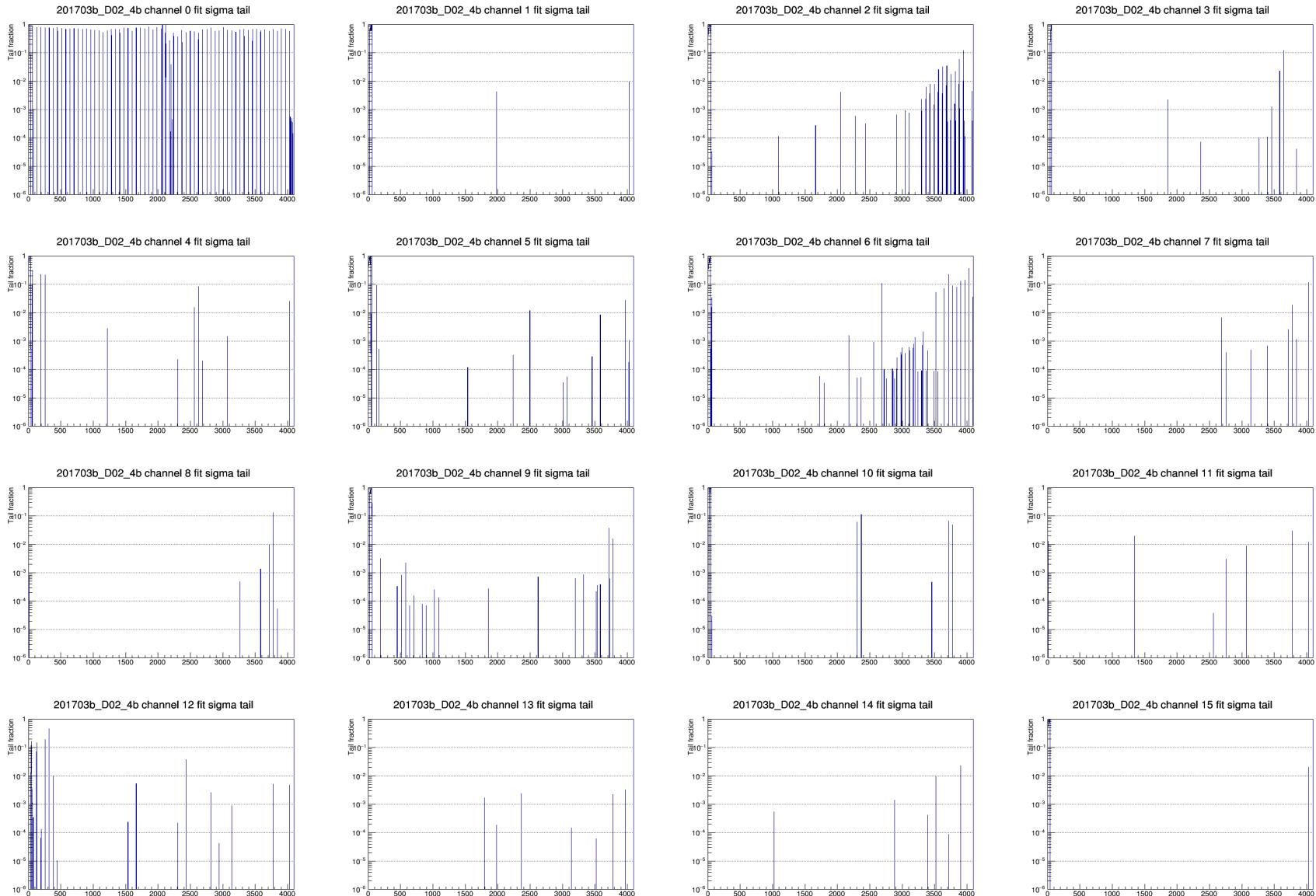
Tails: chip D02, time 3b



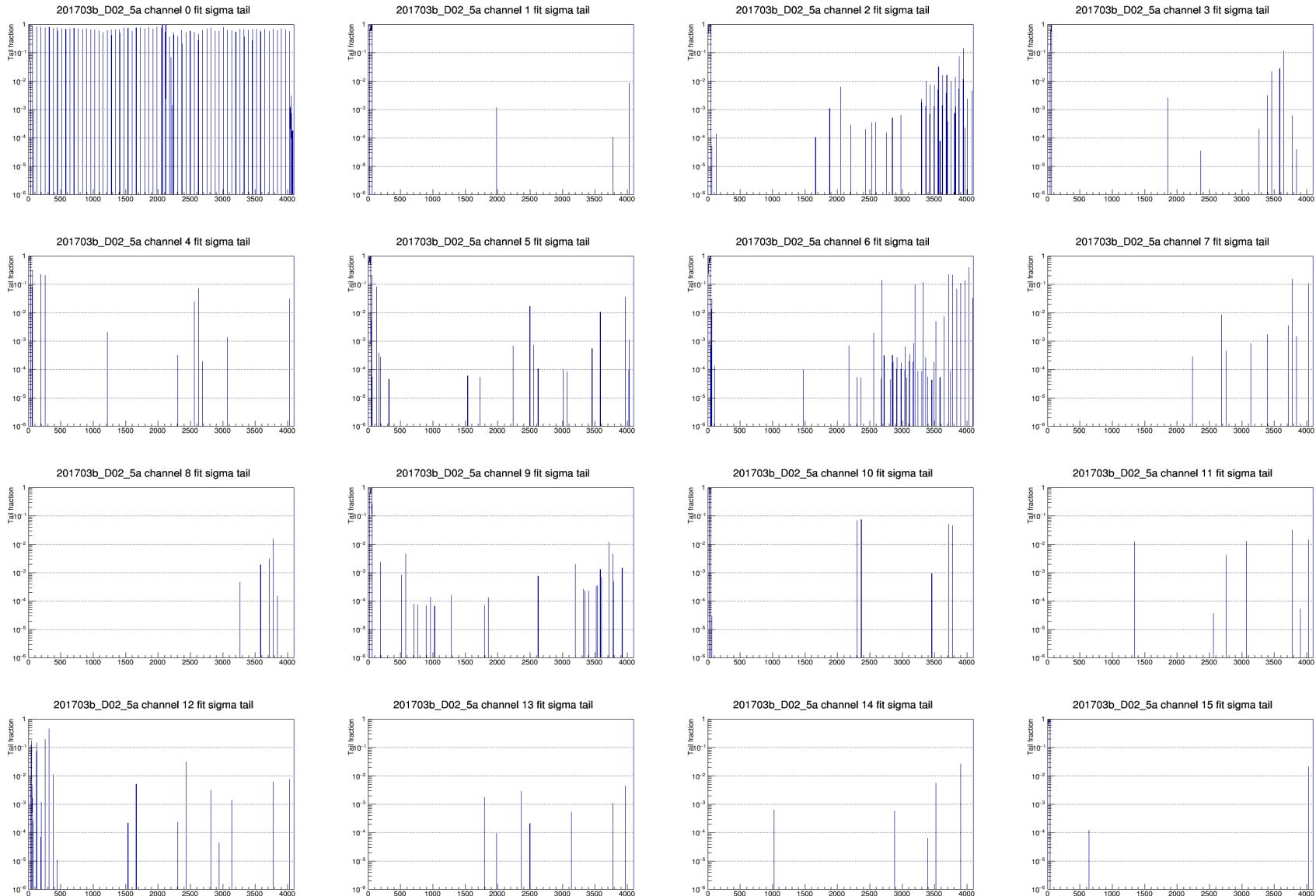
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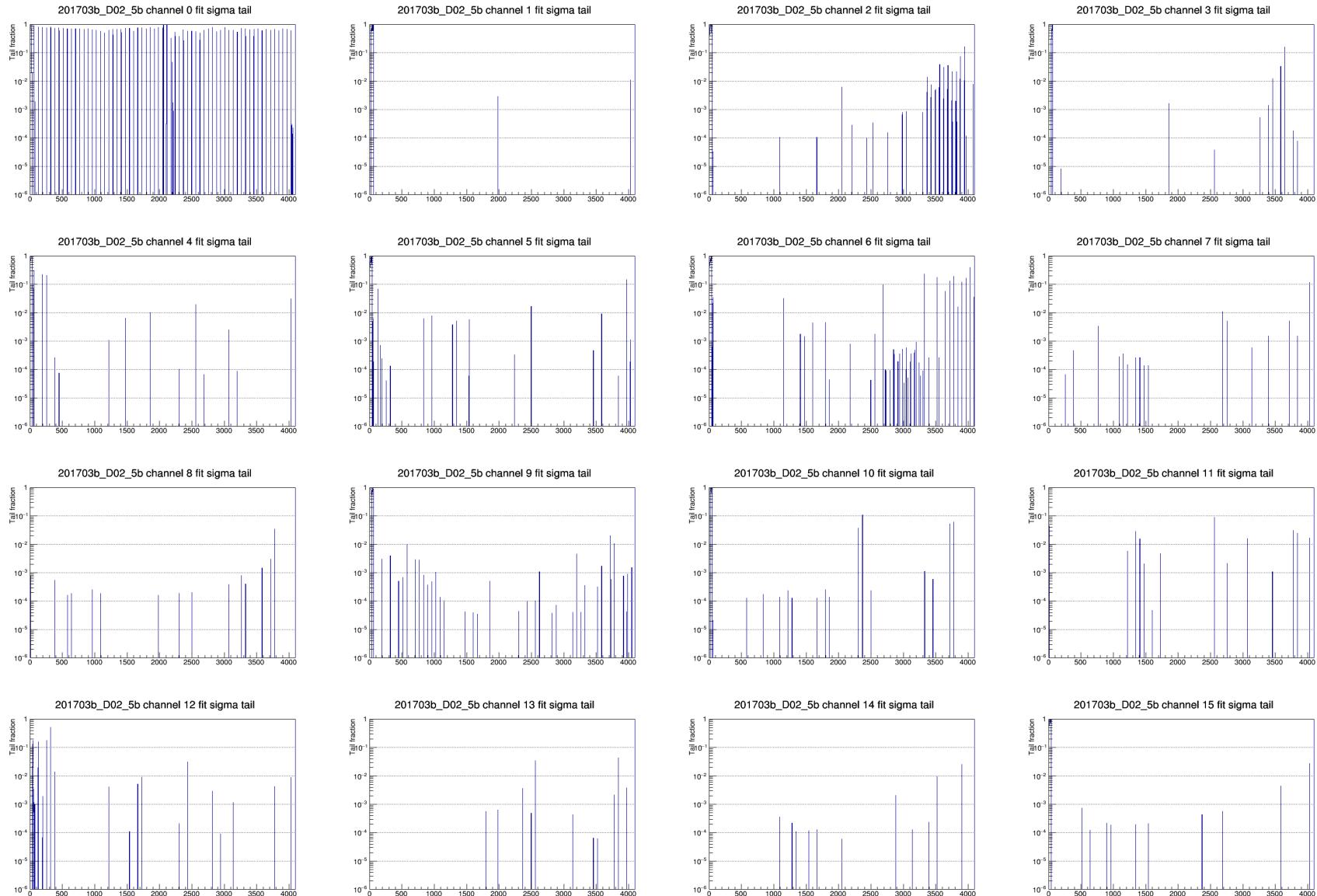
Tails: chip D02, time 4b



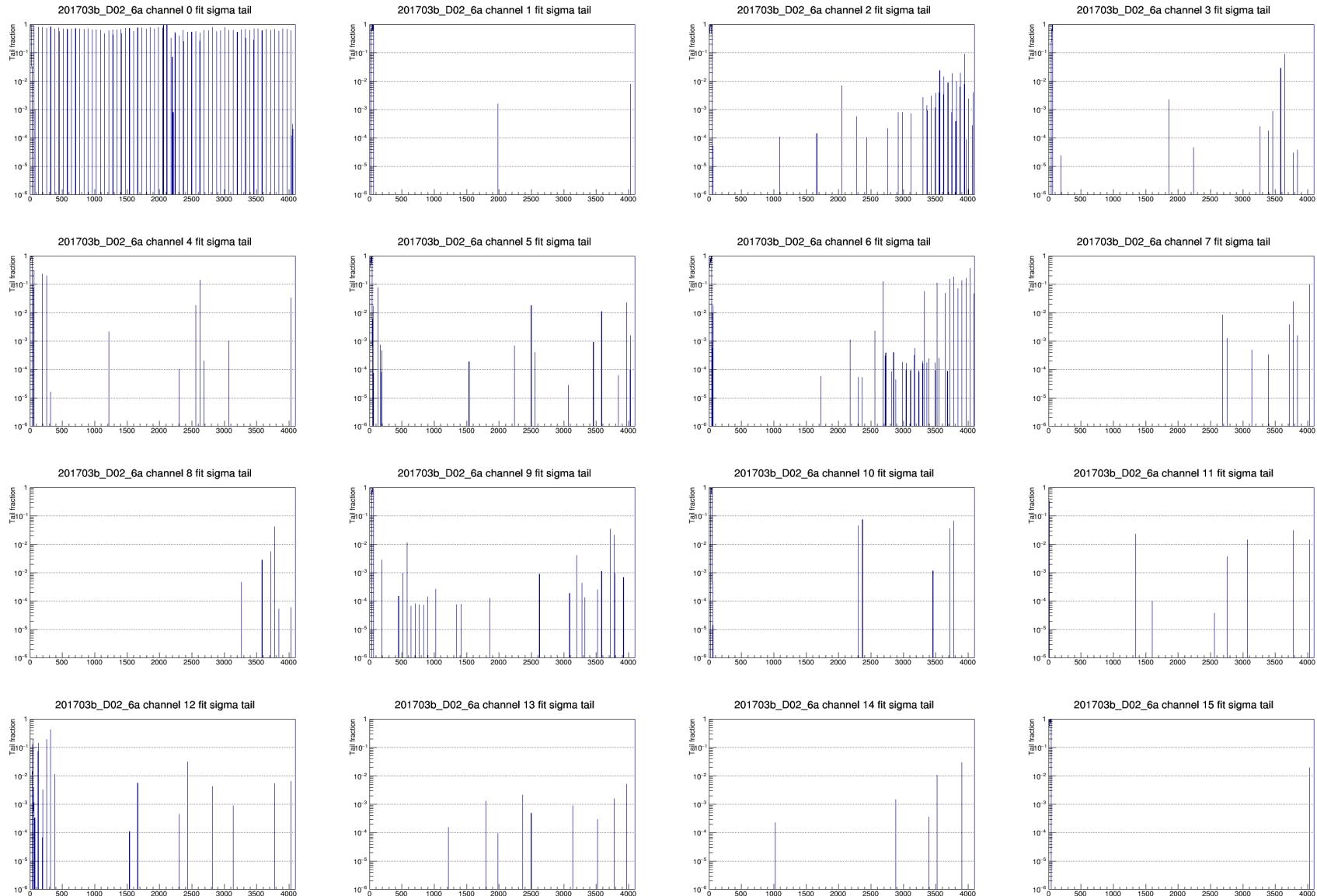
Tails: chip D02, time 5a



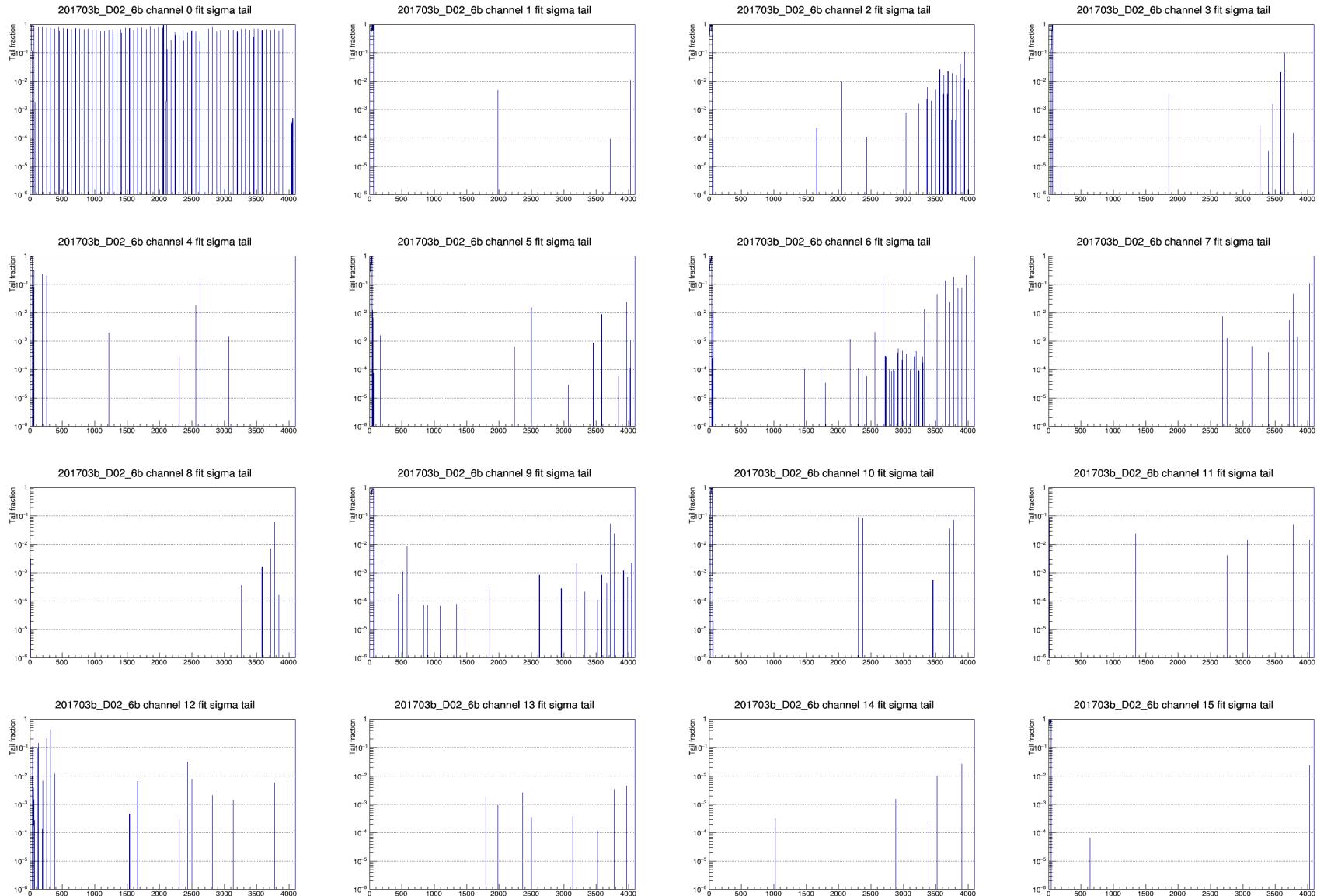
Tails: chip D02, time 5b



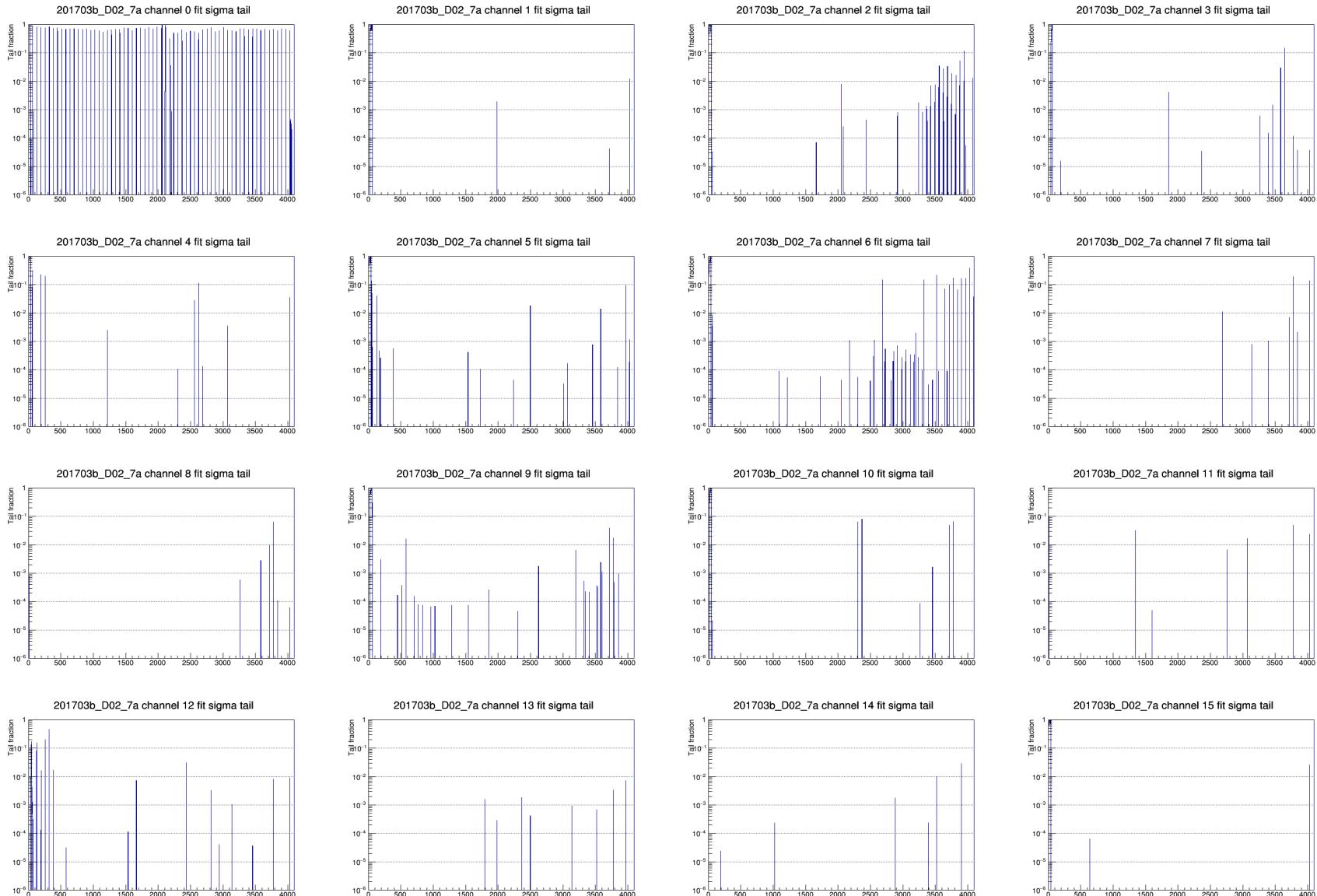
Tails: chip D02, time 6a



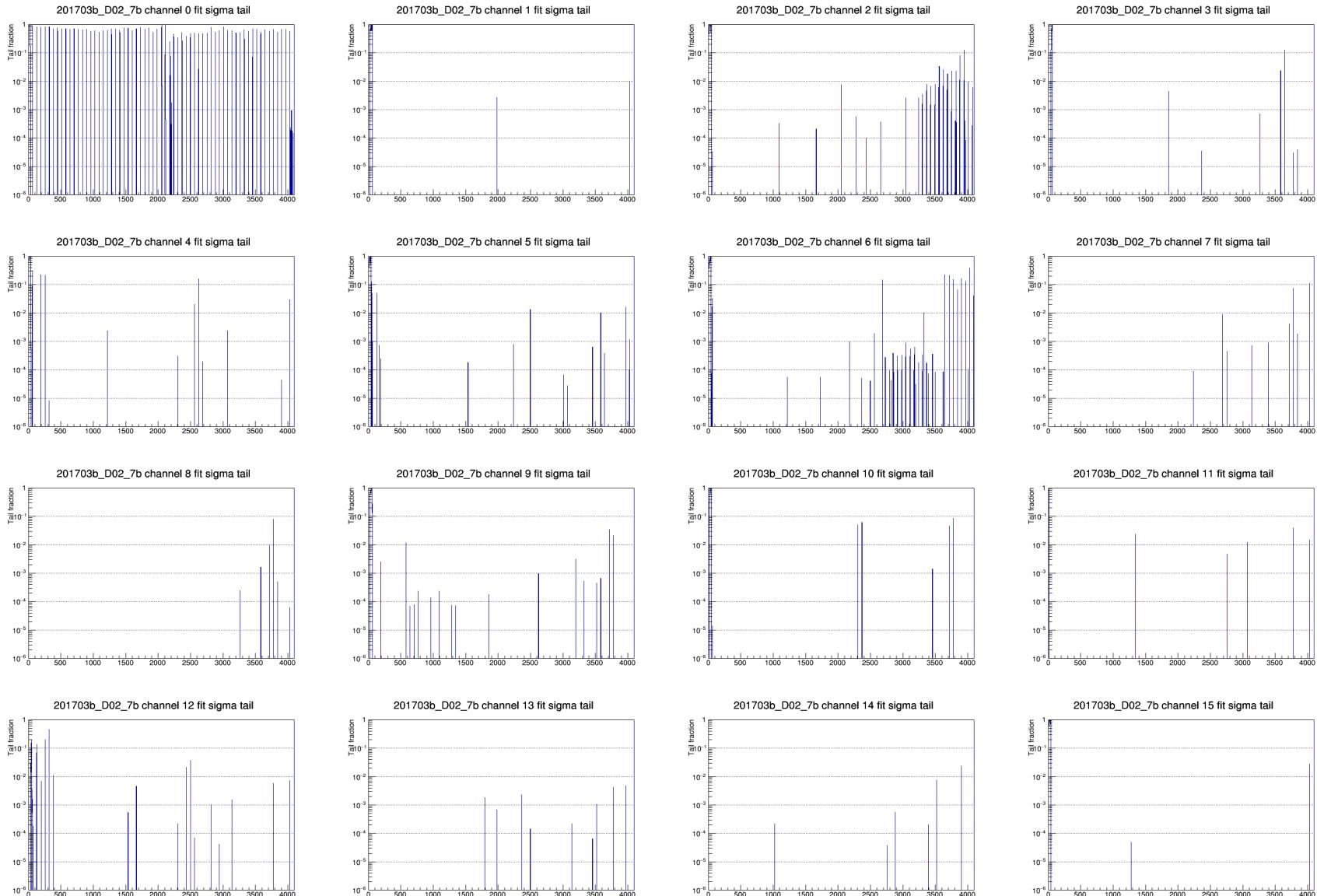
Tails: chip D02, time 6b



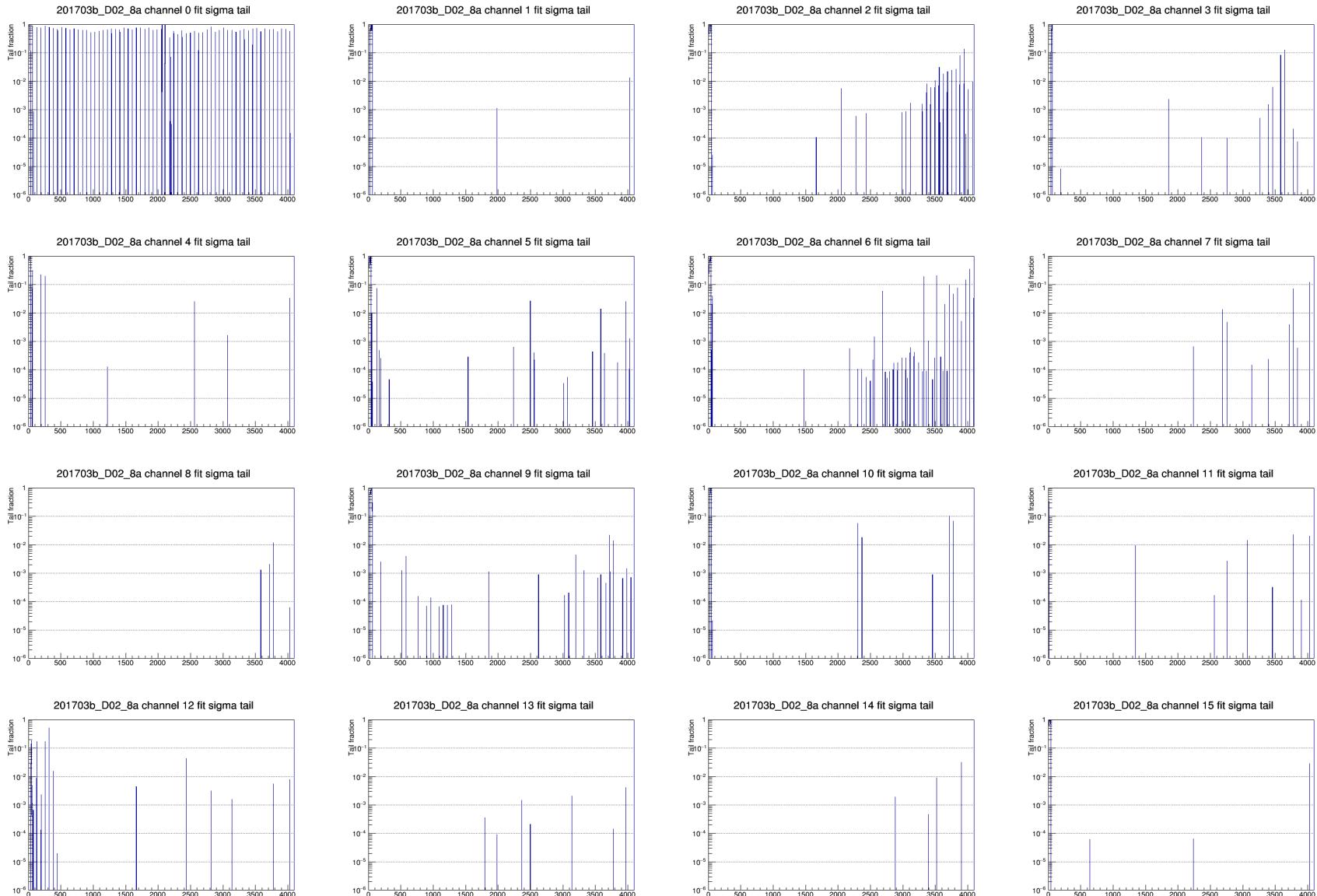
Tails: chip D02, time 7a



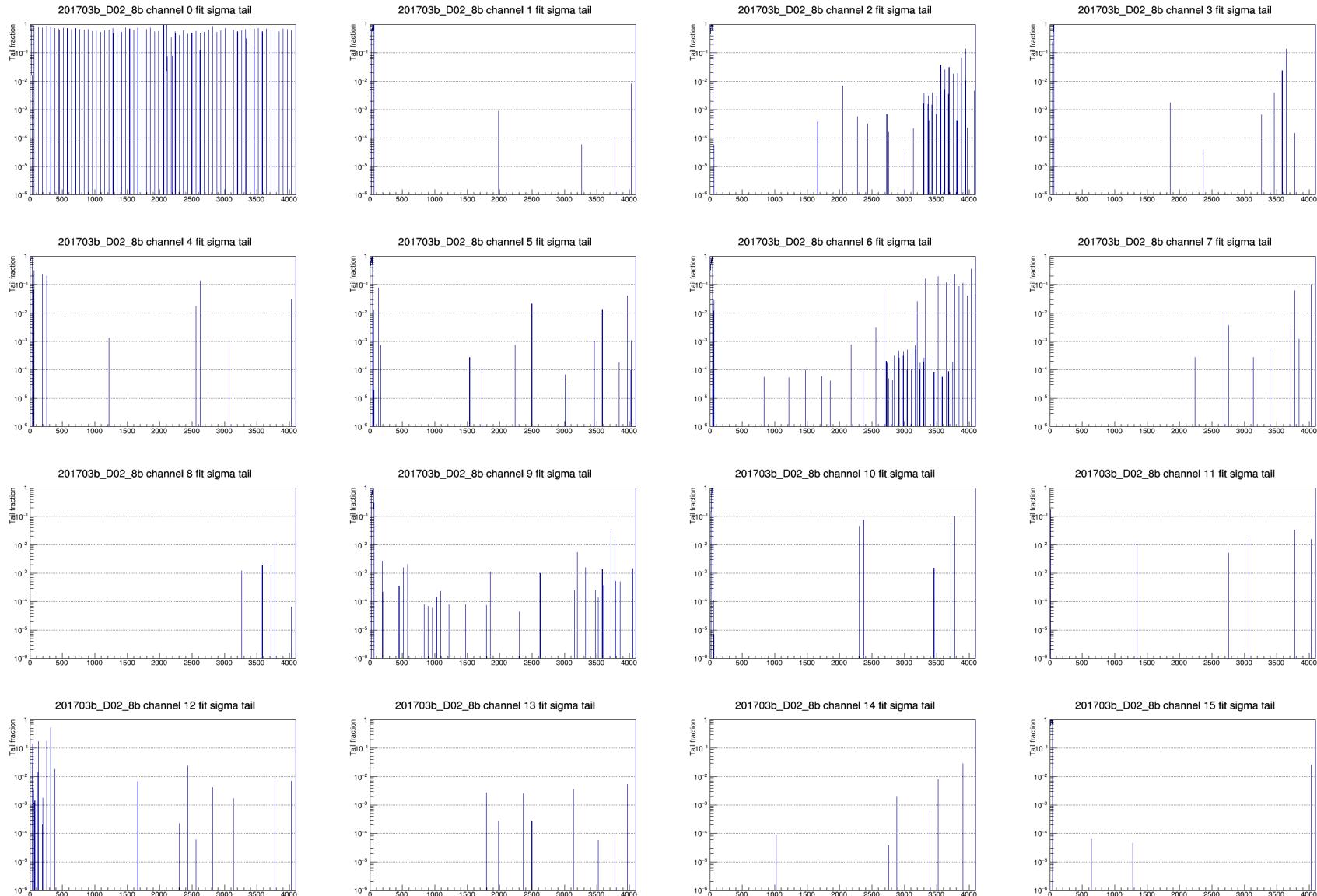
Tails: chip D02, time 7b



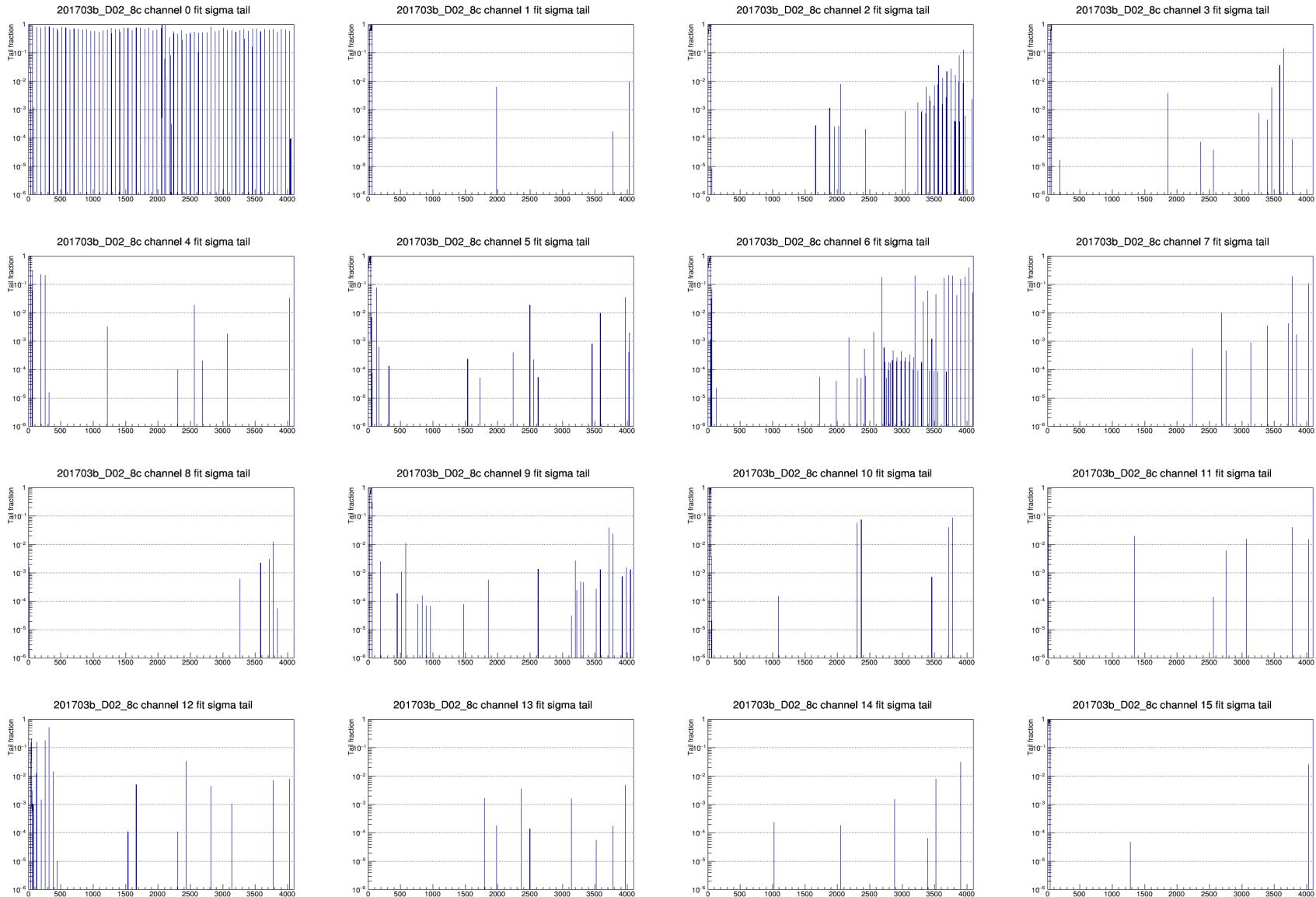
Tails: chip D02, time 8a



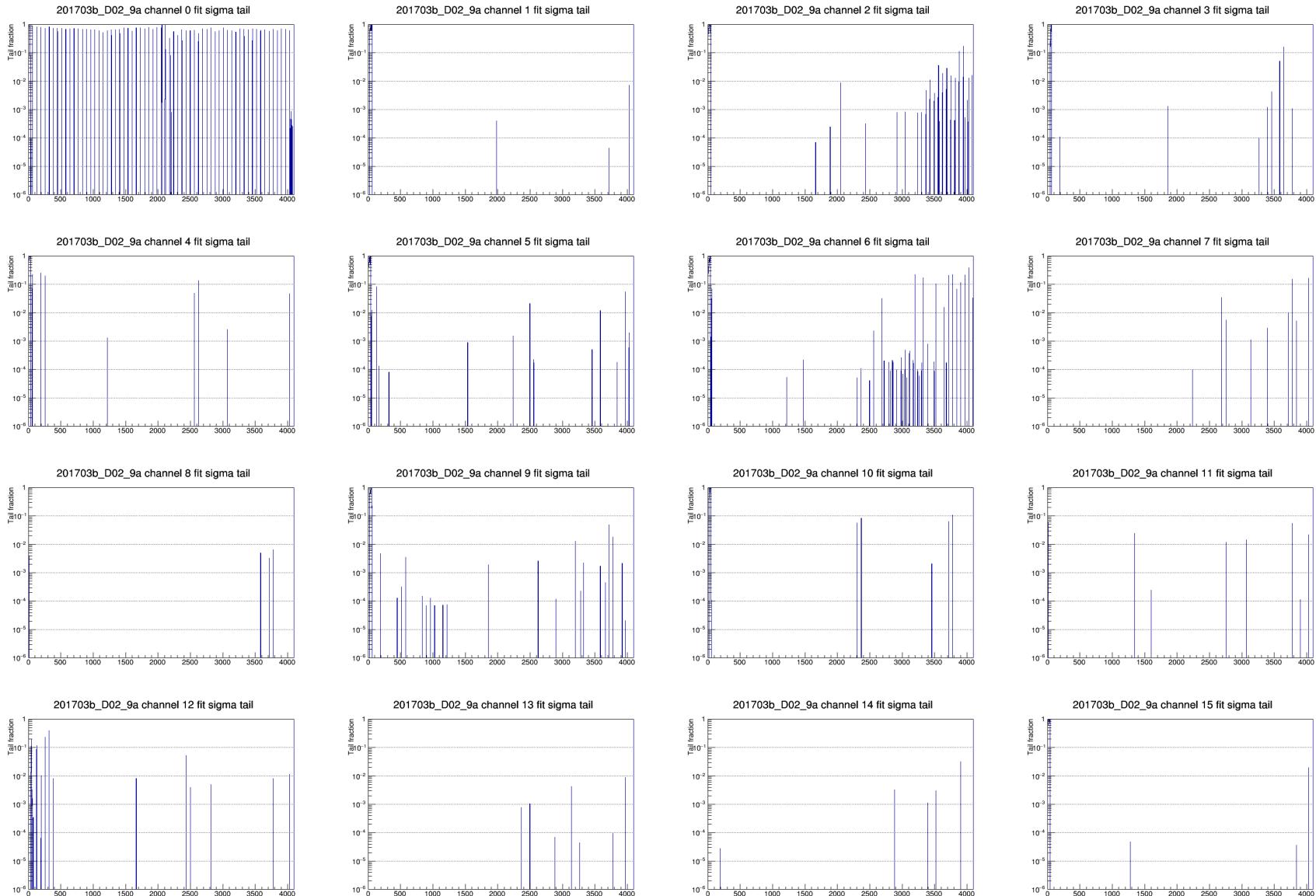
Tails: chip D02, time 8b



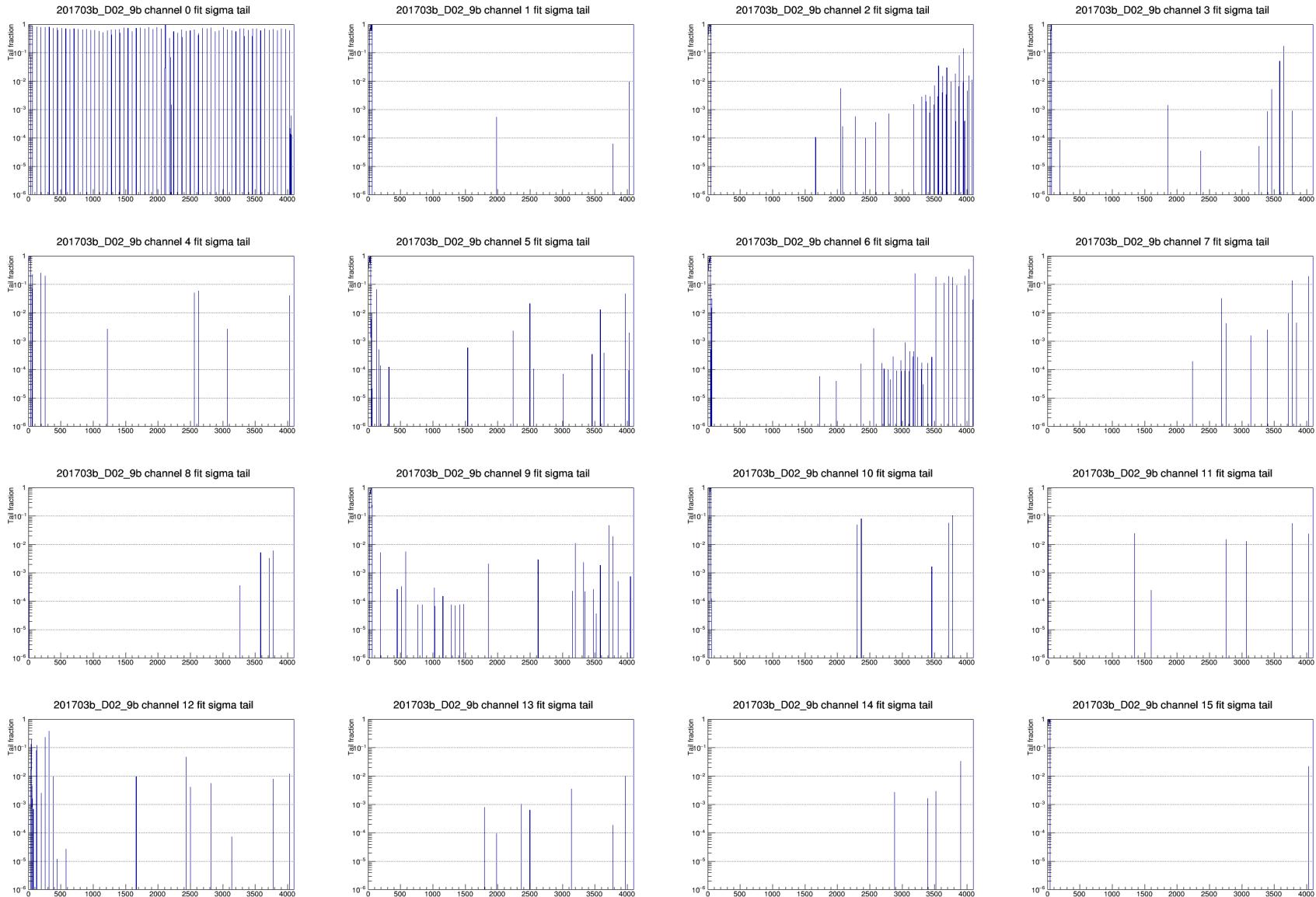
Tails: chip D02, time 8c



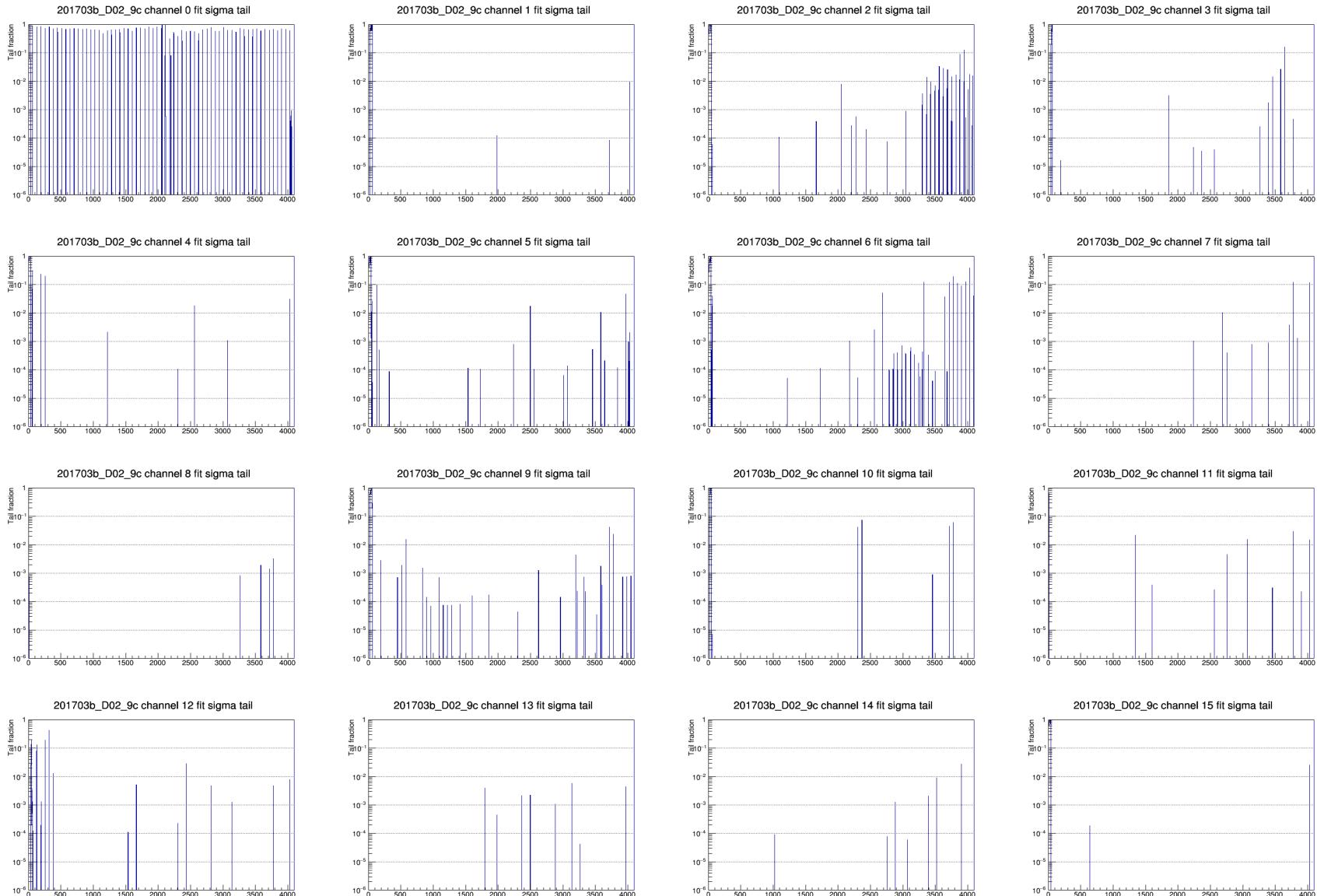
Tails: chip D02, time 9a



Tails: chip D02, time 9b

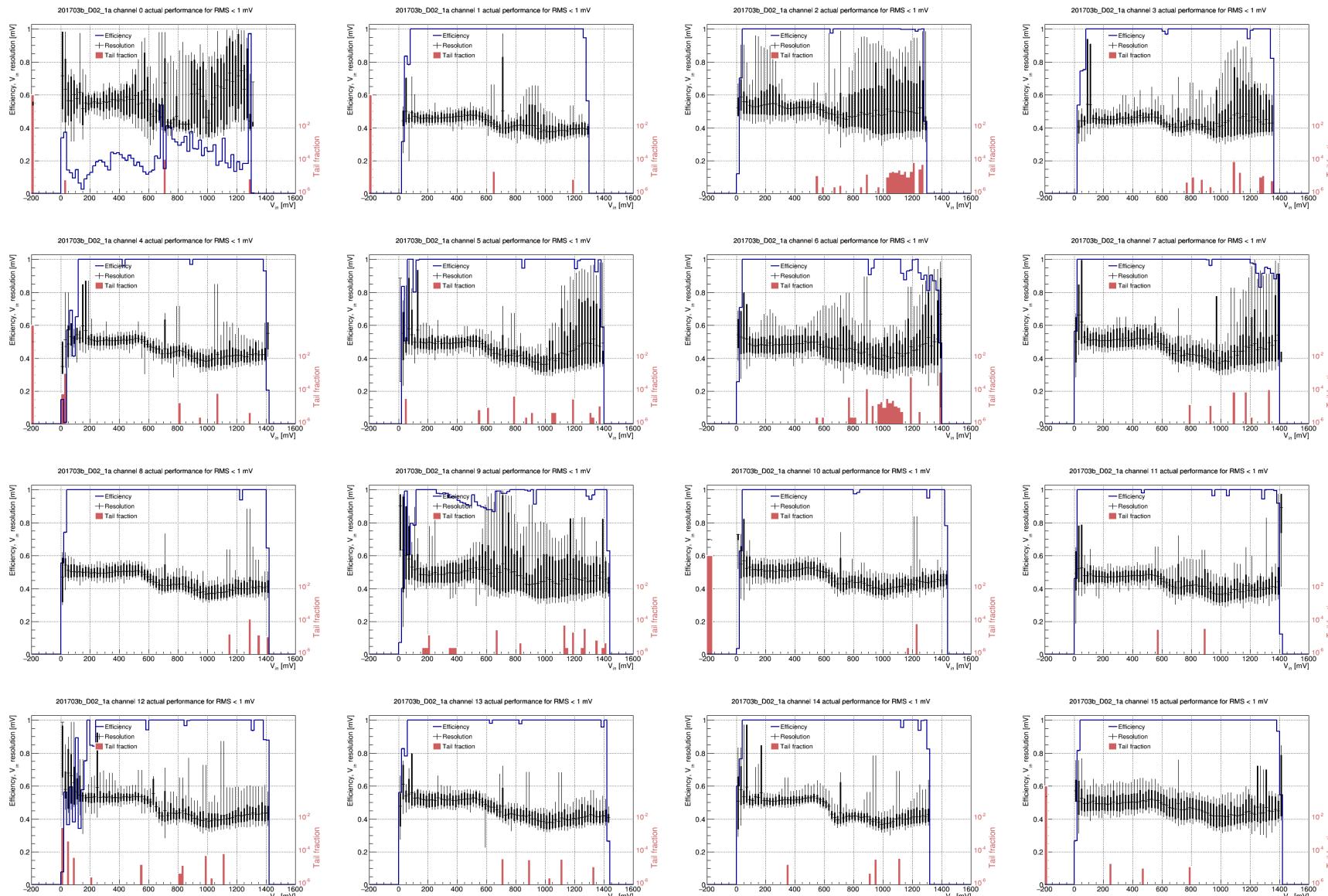


Tails: chip D02, time 9c

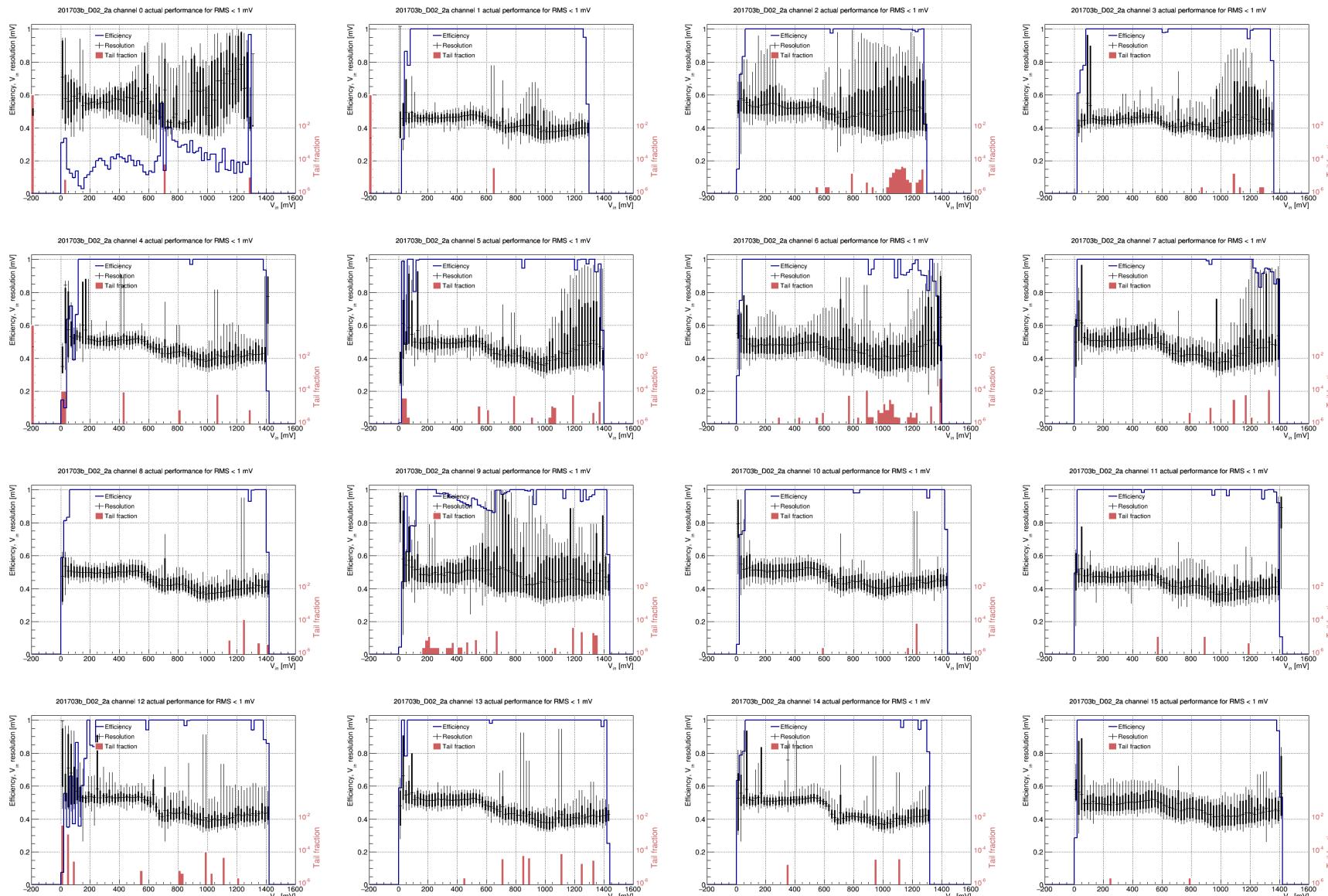


Performance

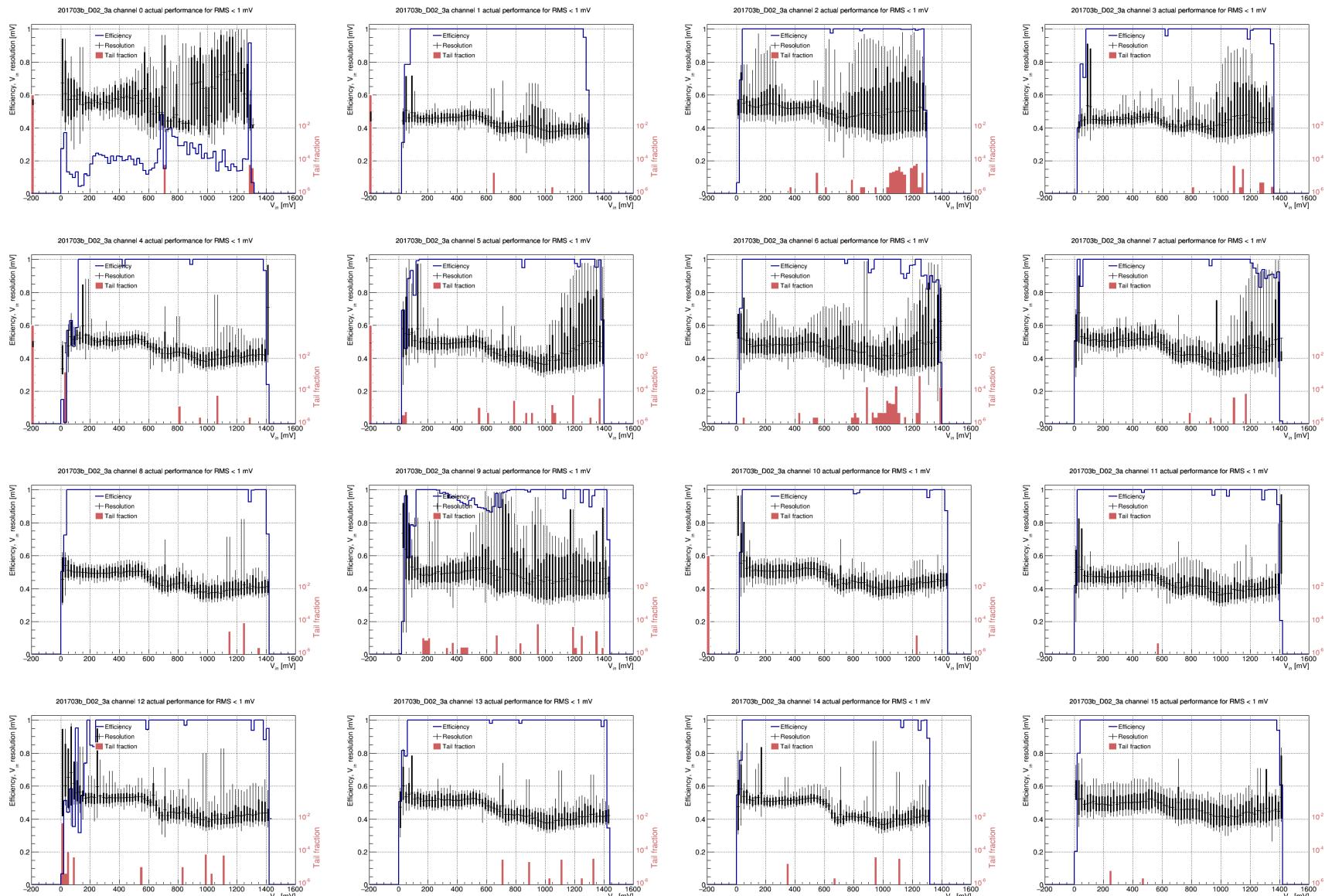
Performance: chip D02, time 1a



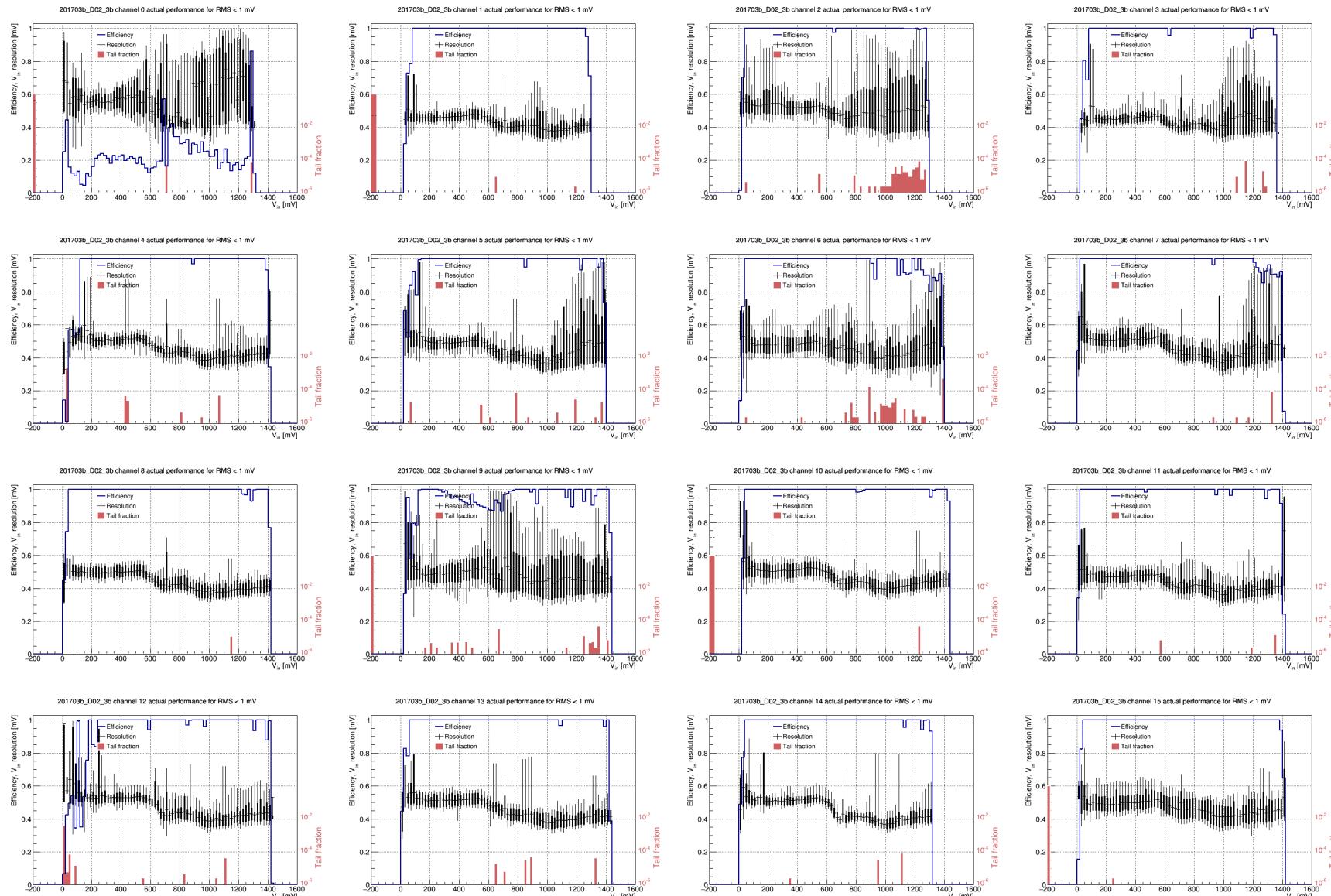
Performance: chip D02, time 2a



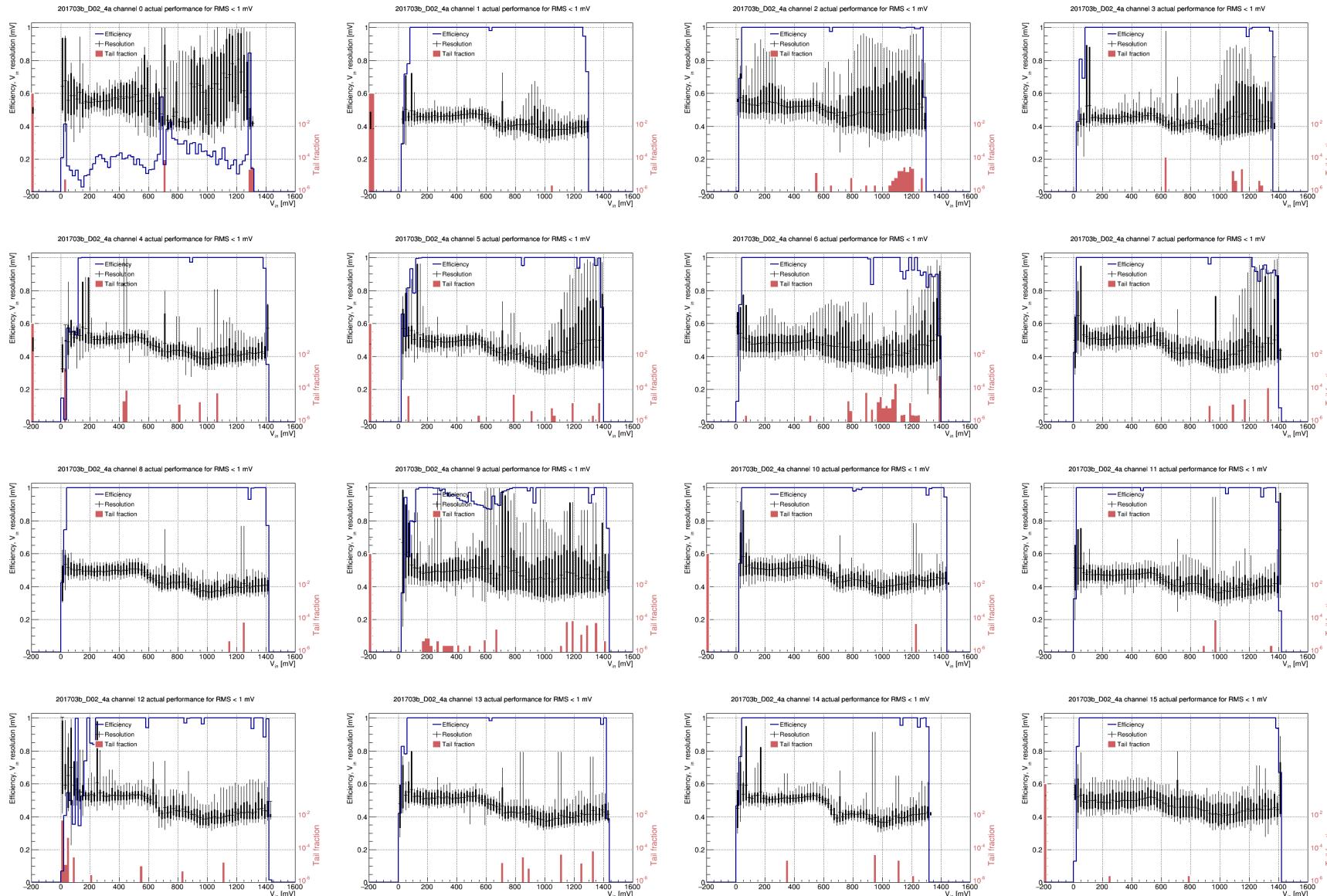
Performance: chip D02, time 3a



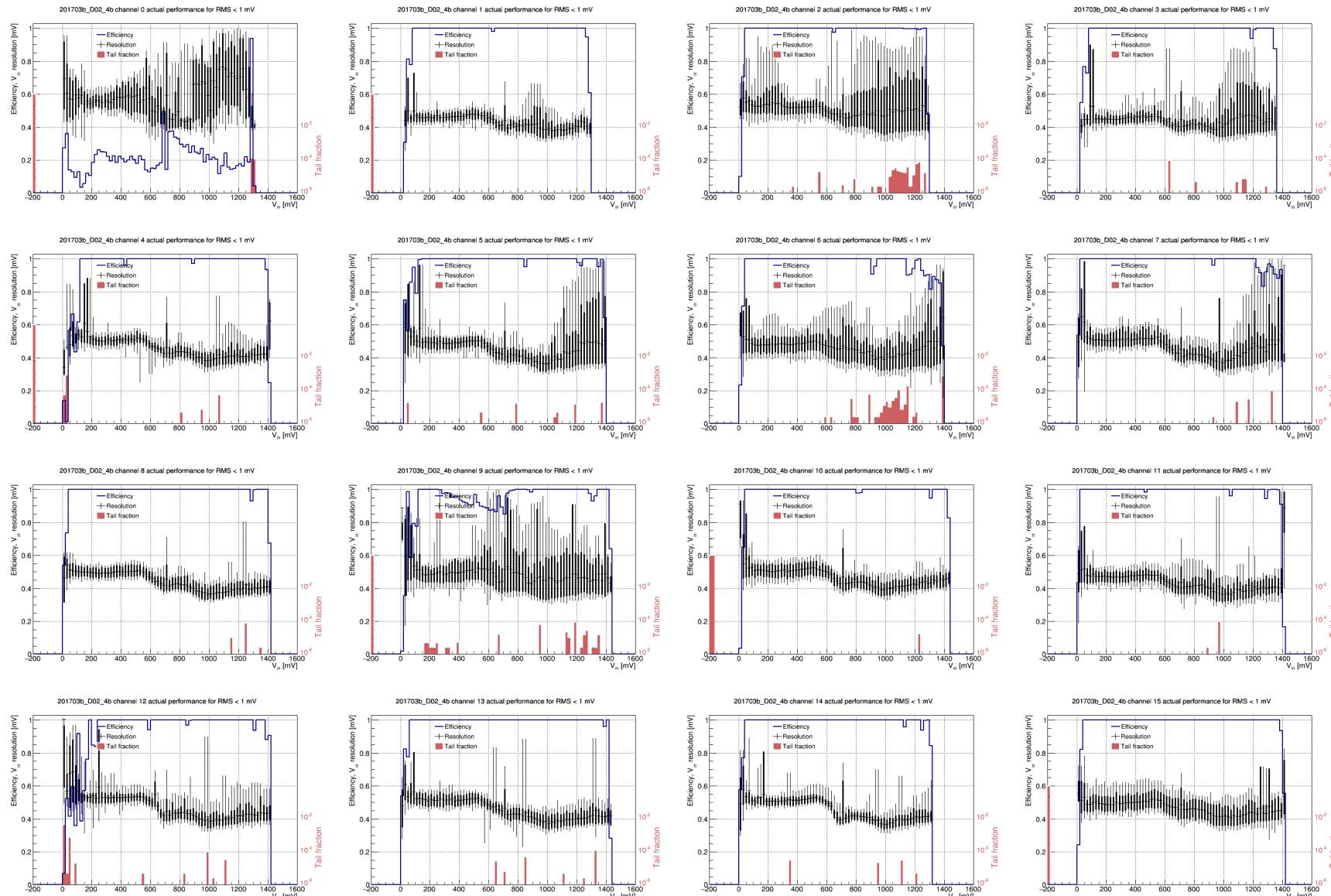
Performance: chip D02, time 3b



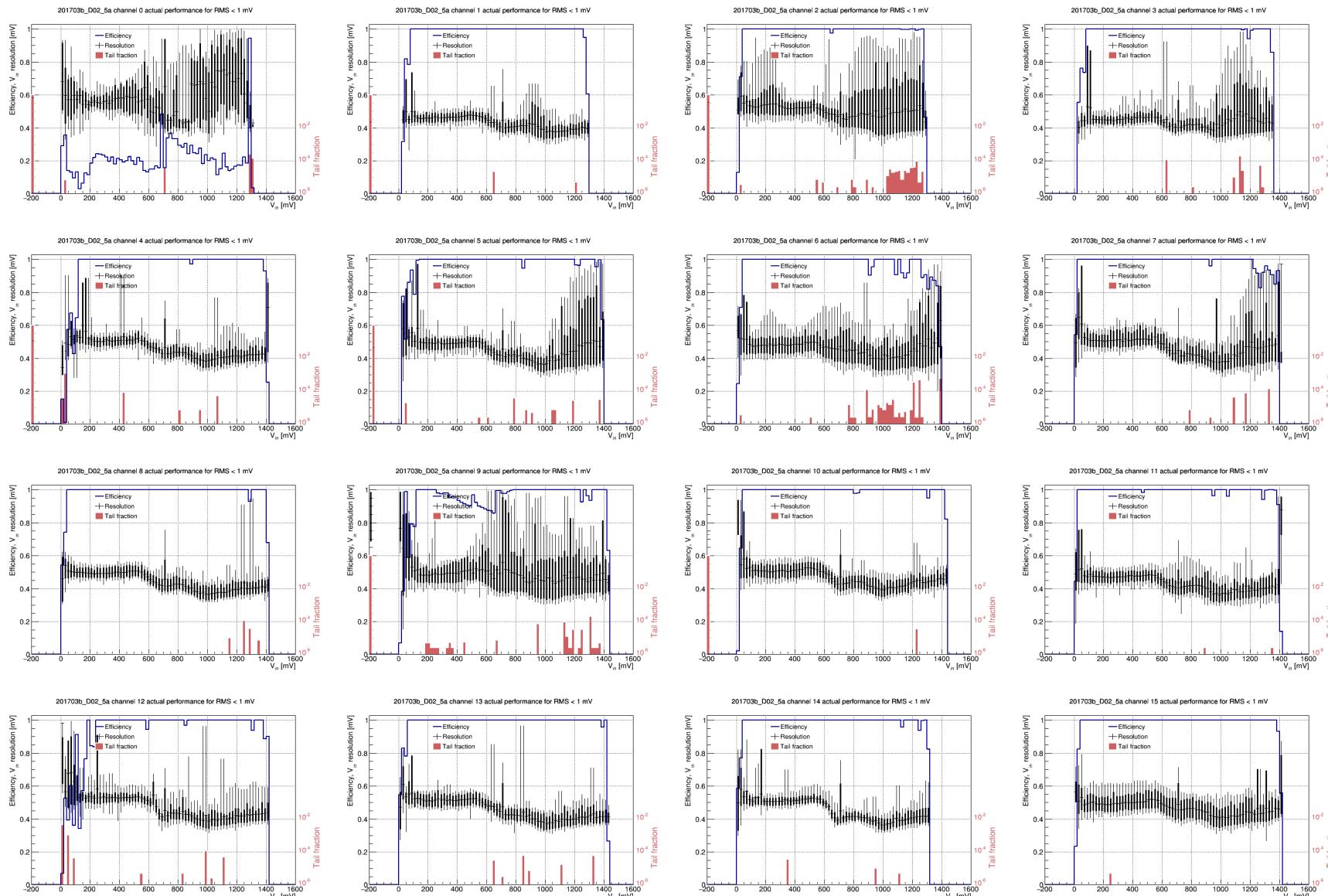
Performance: chip D02, time 4a



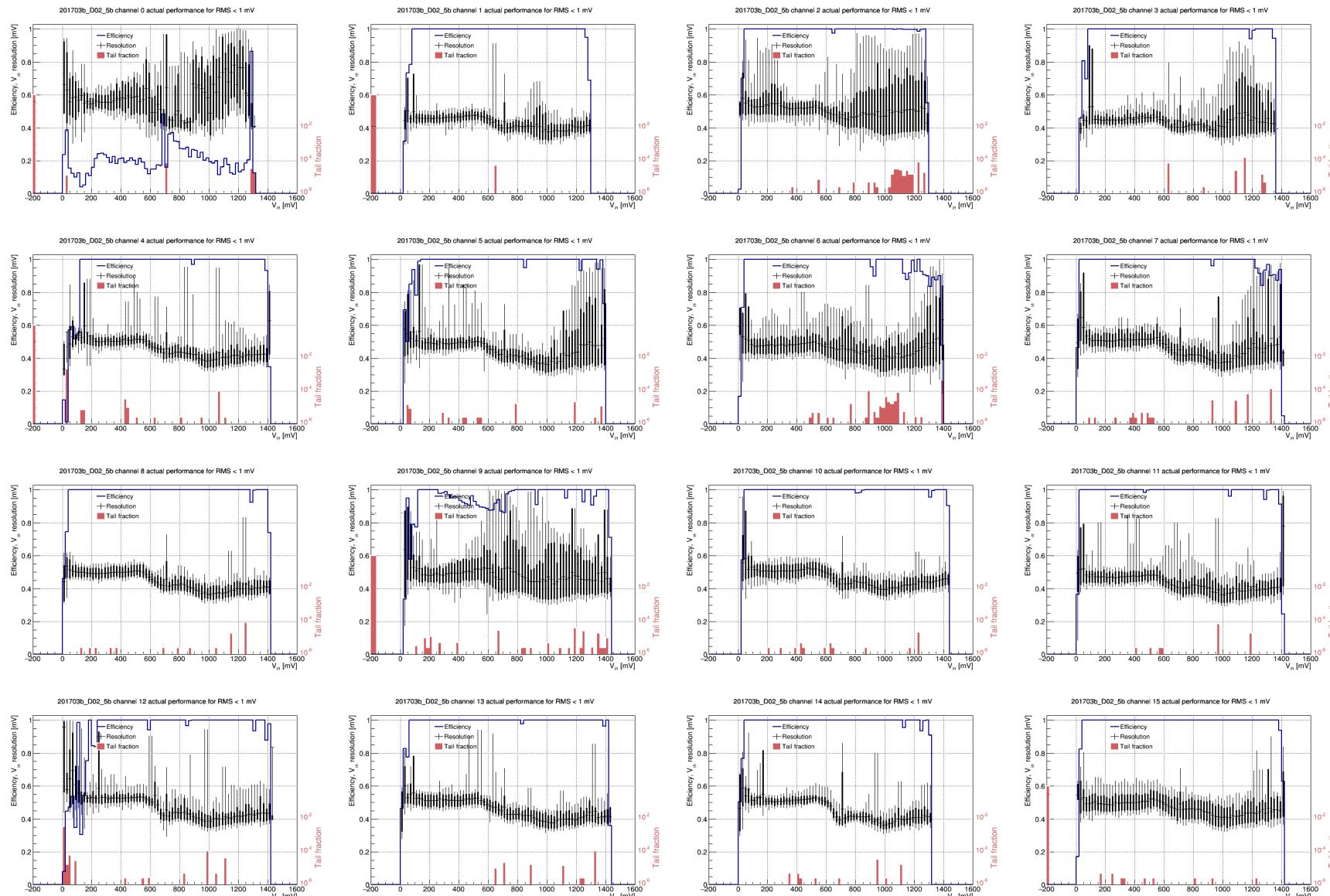
Performance: chip D02, time 4b



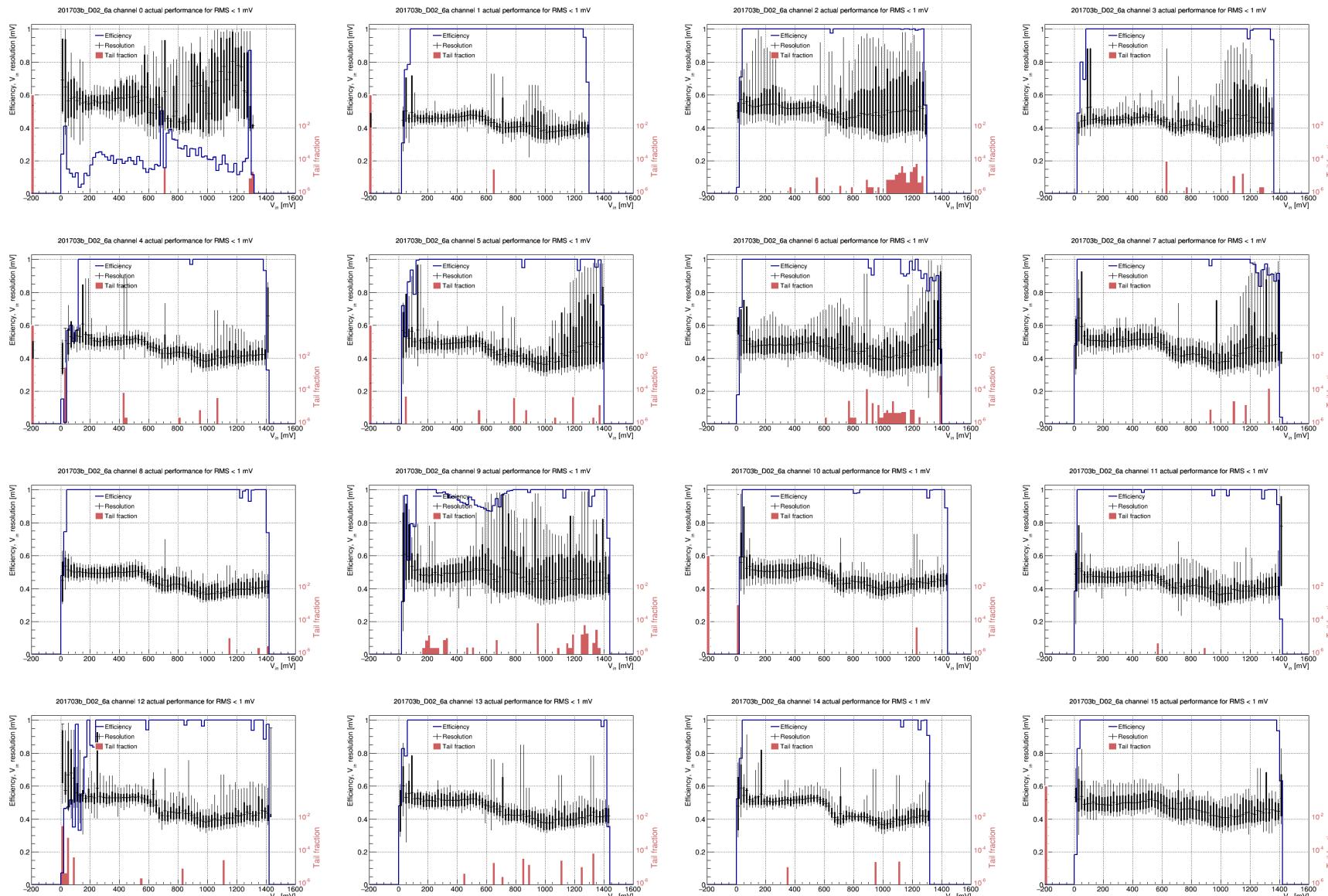
Performance: chip D02, time 5a



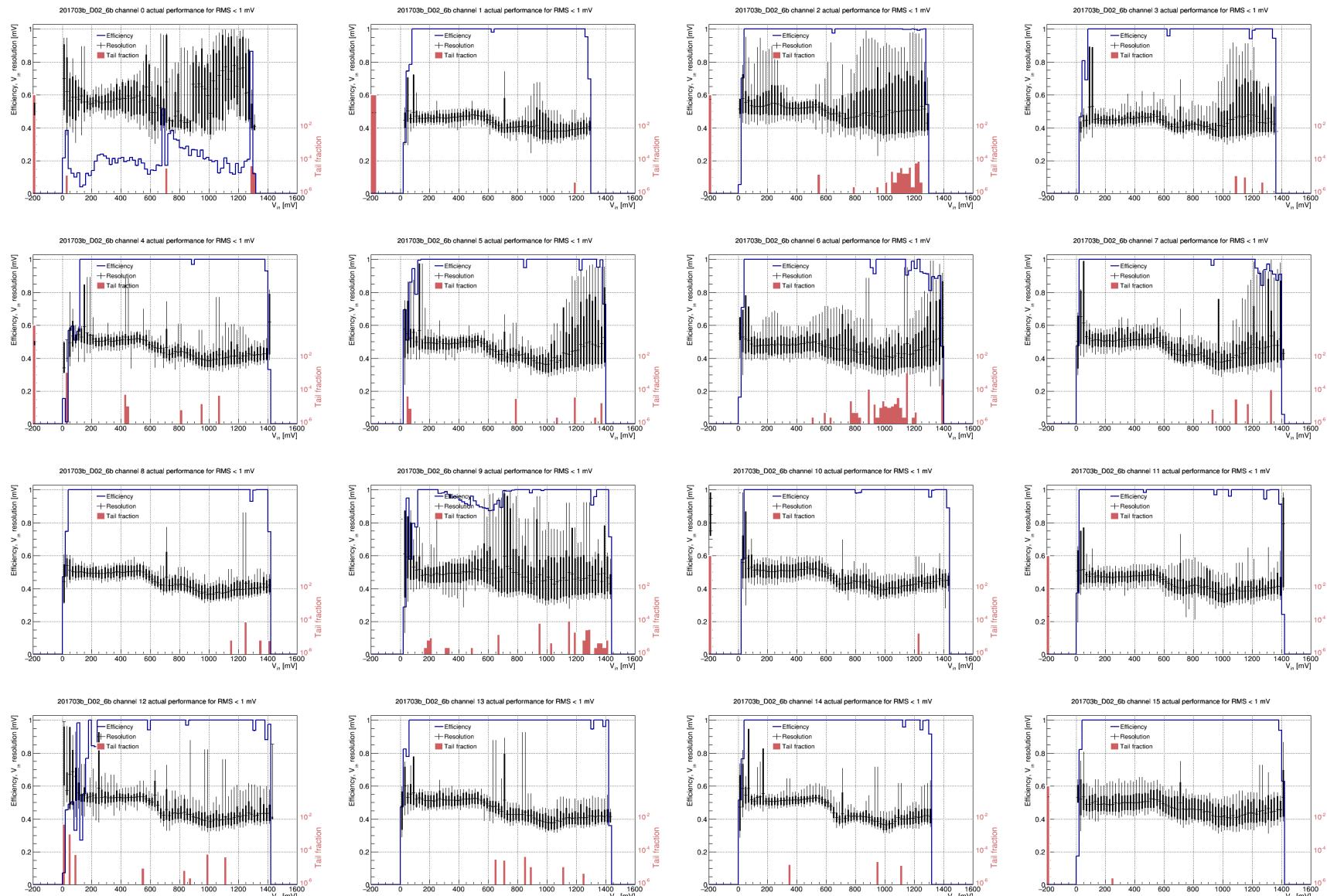
Performance: chip D02, time 5b



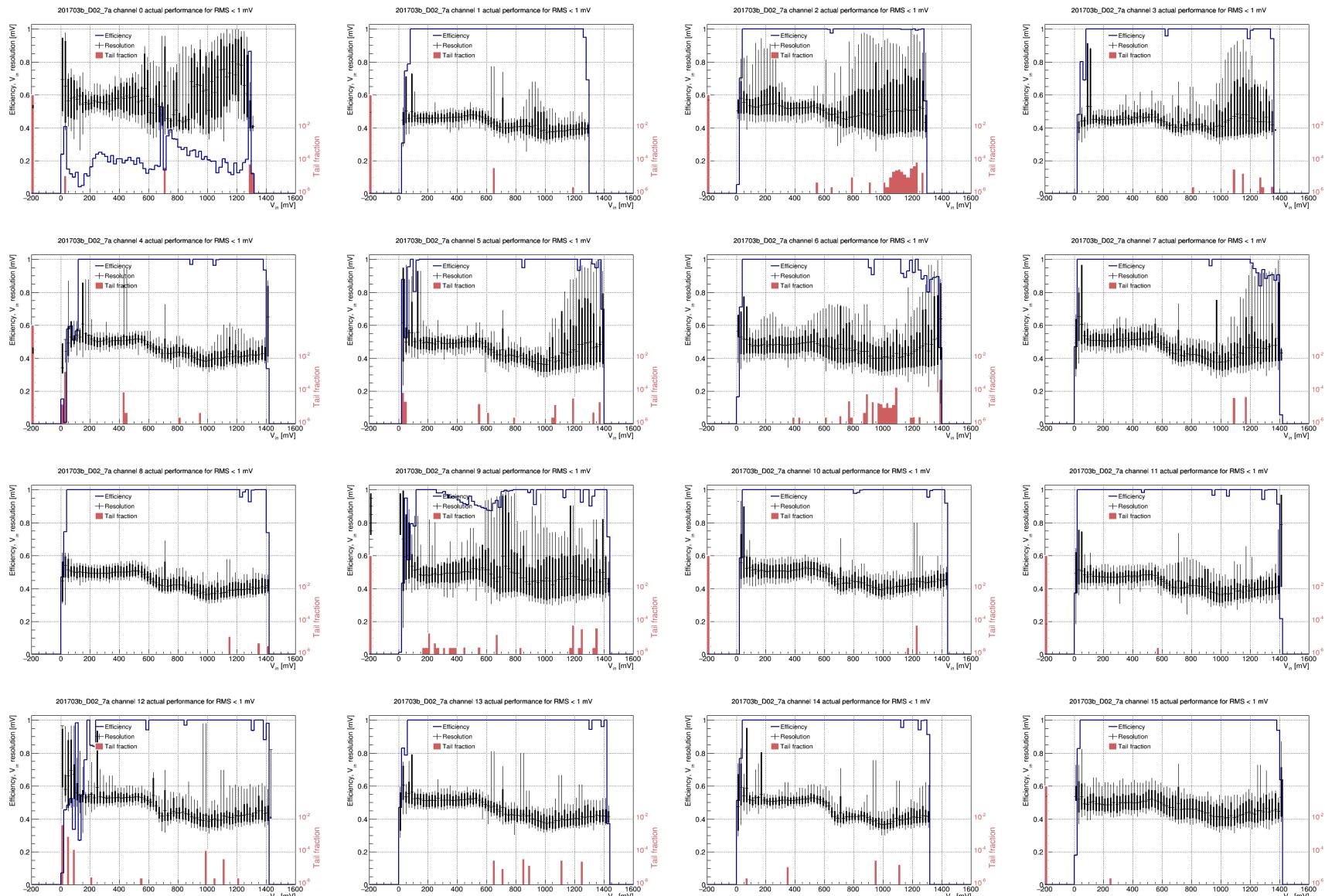
Performance: chip D02, time 6a



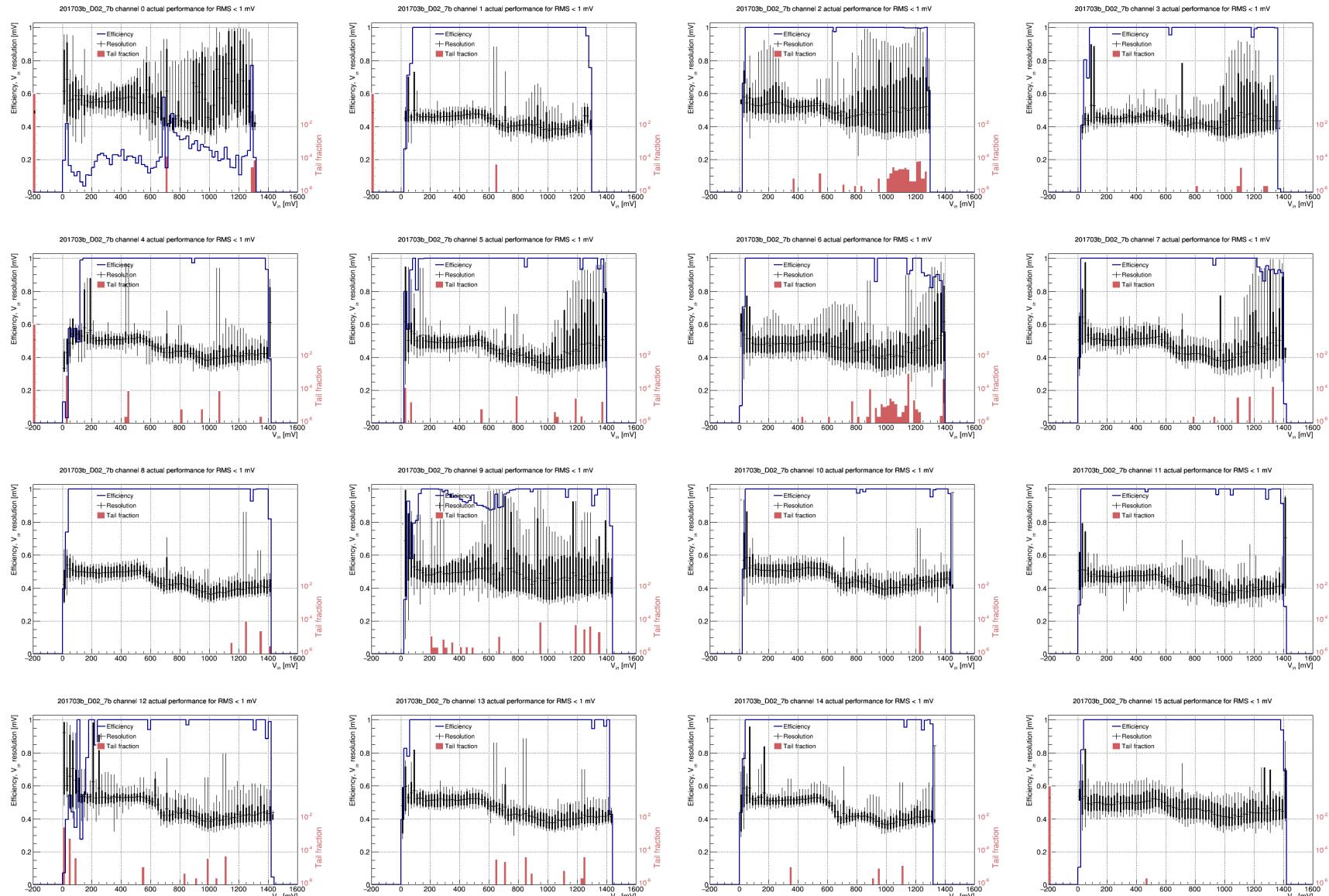
Performance: chip D02, time 6b



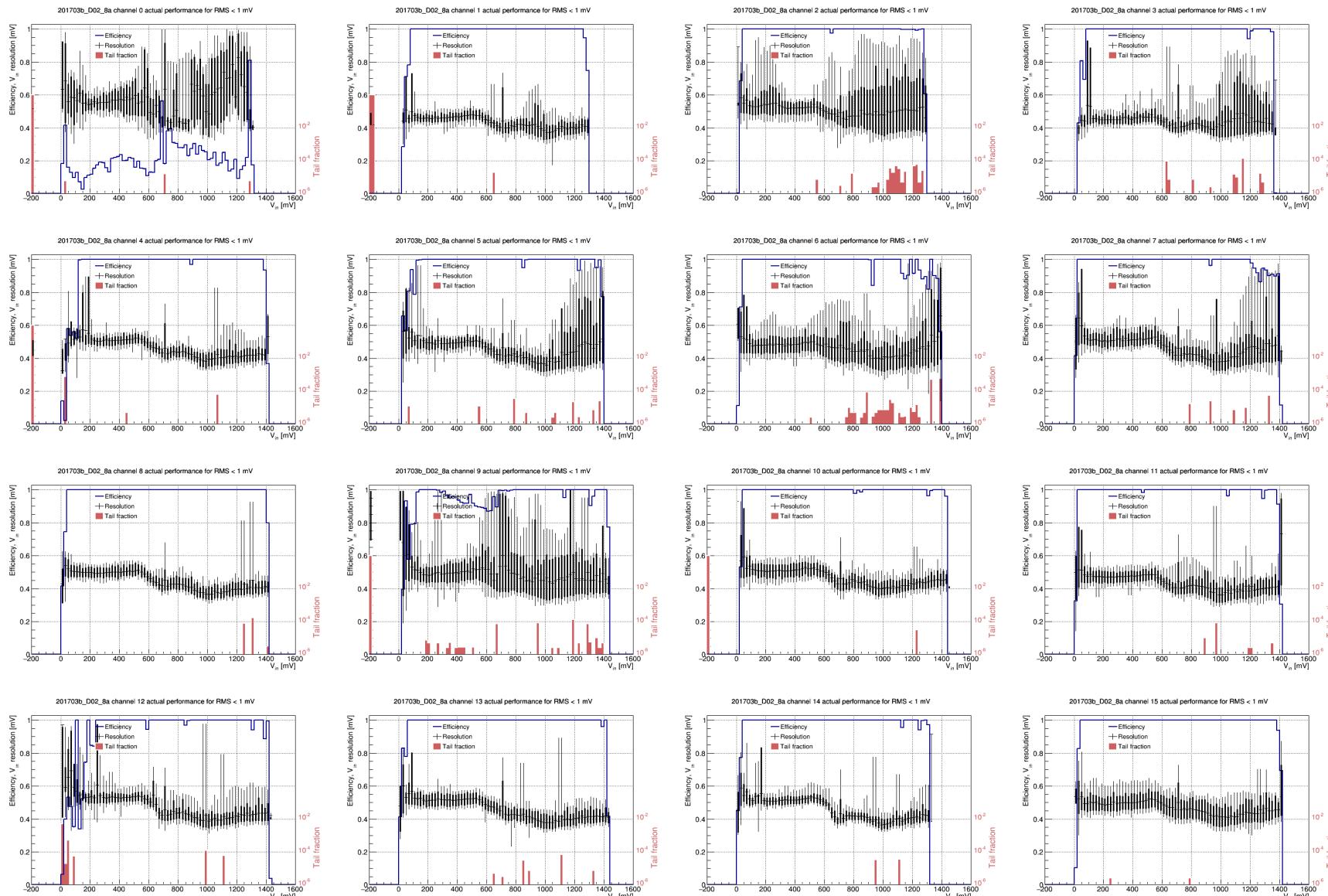
Performance: chip D02, time 7a



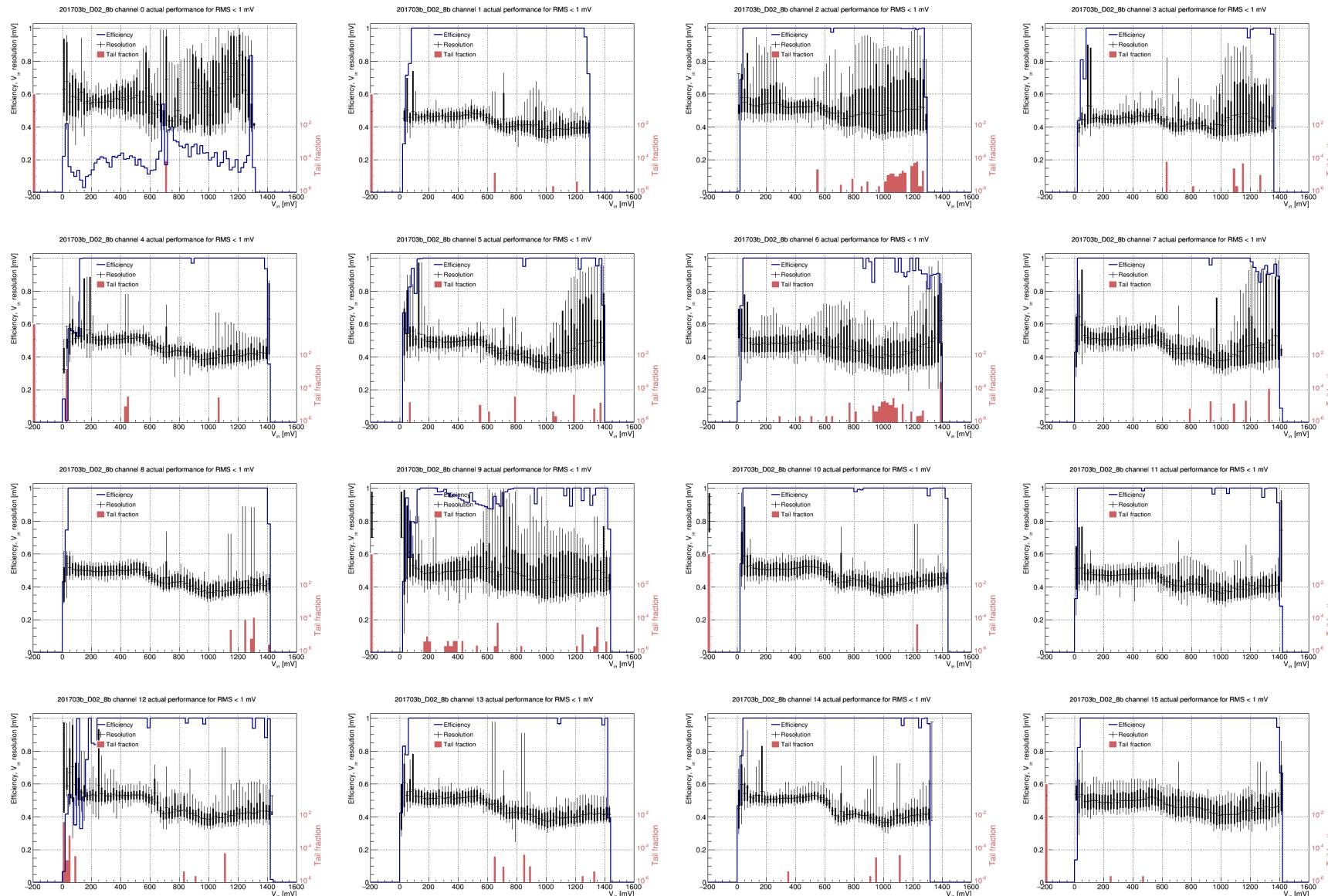
Performance: chip D02, time 7b



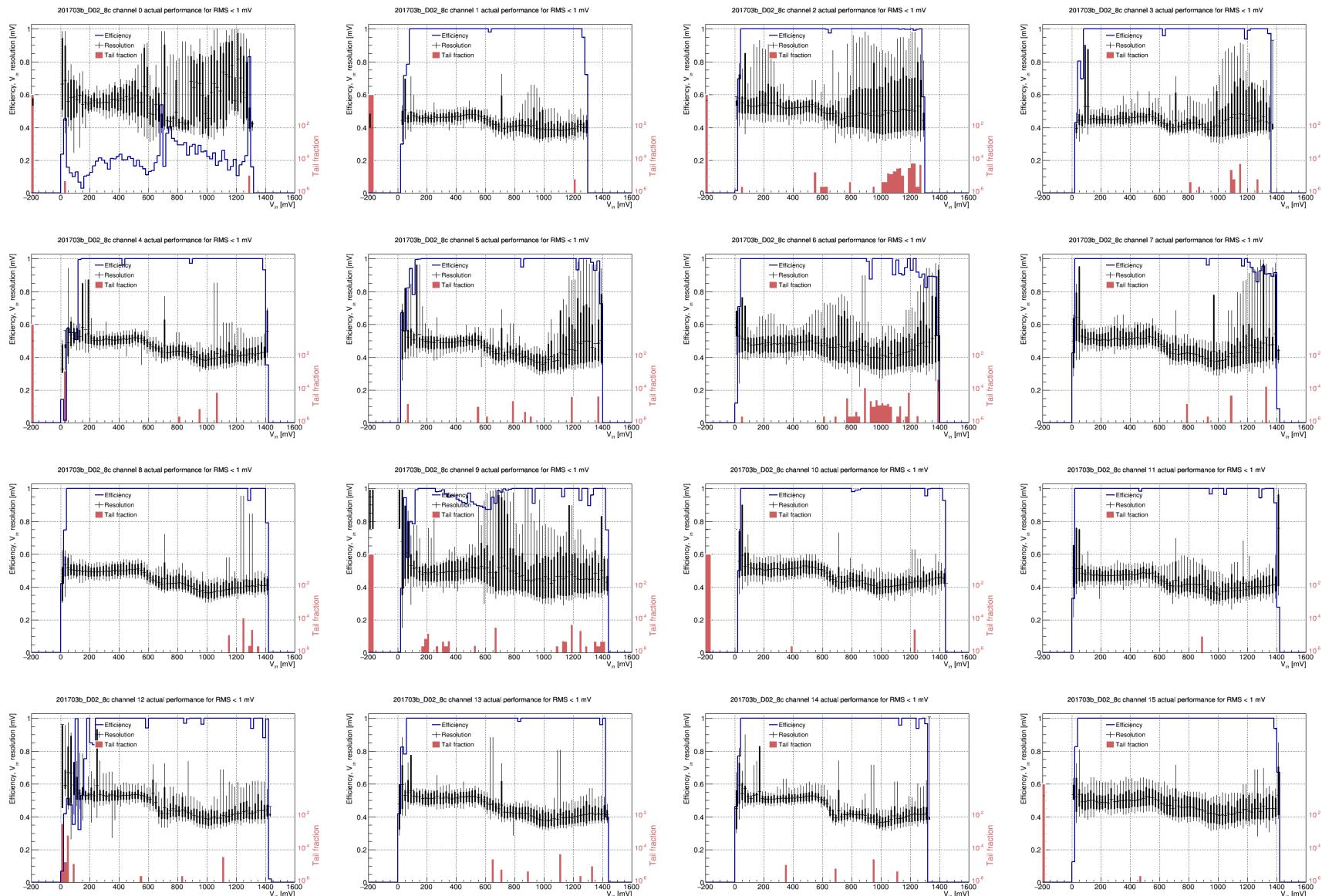
Performance: chip D02, time 8a



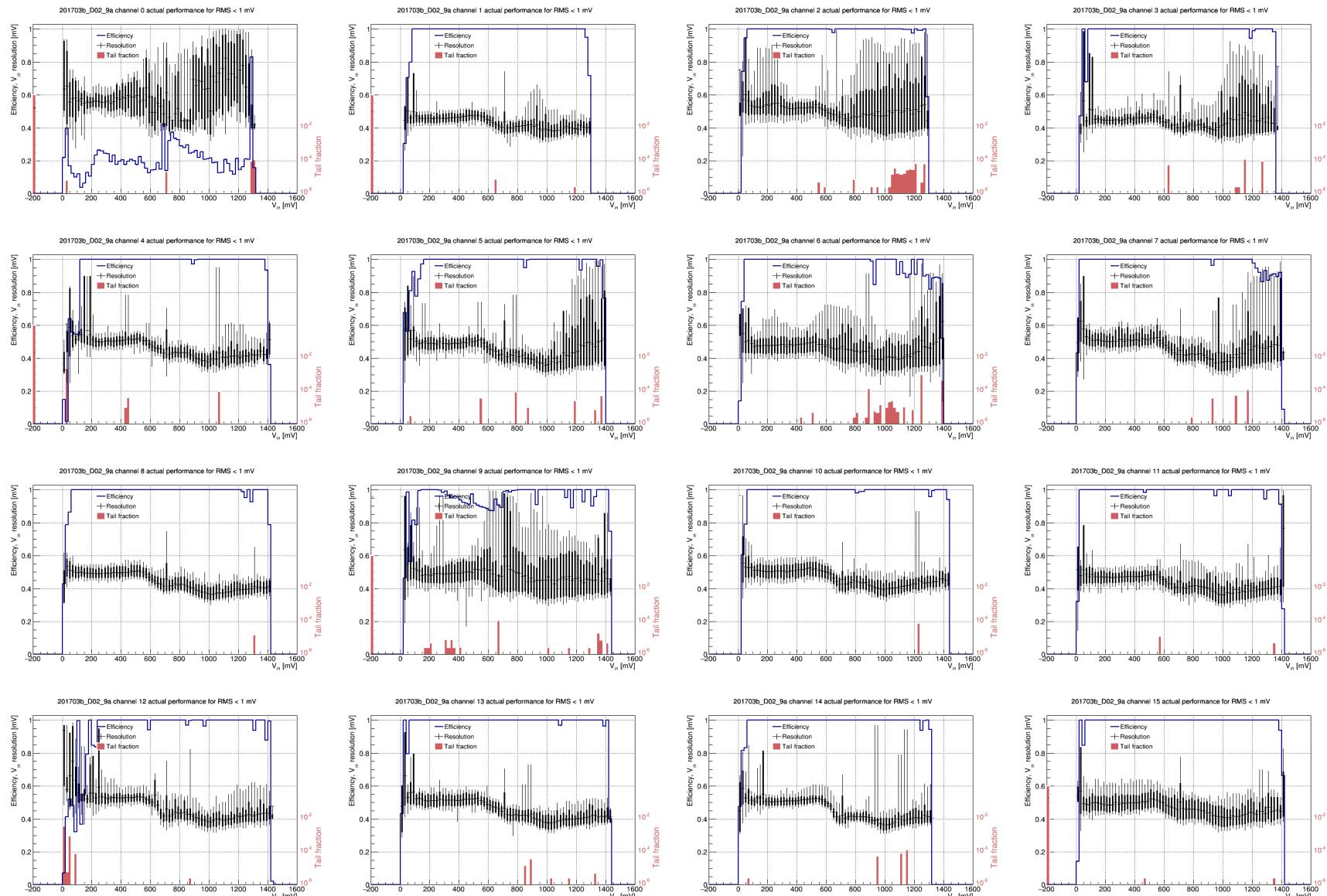
Performance: chip D02, time 8b



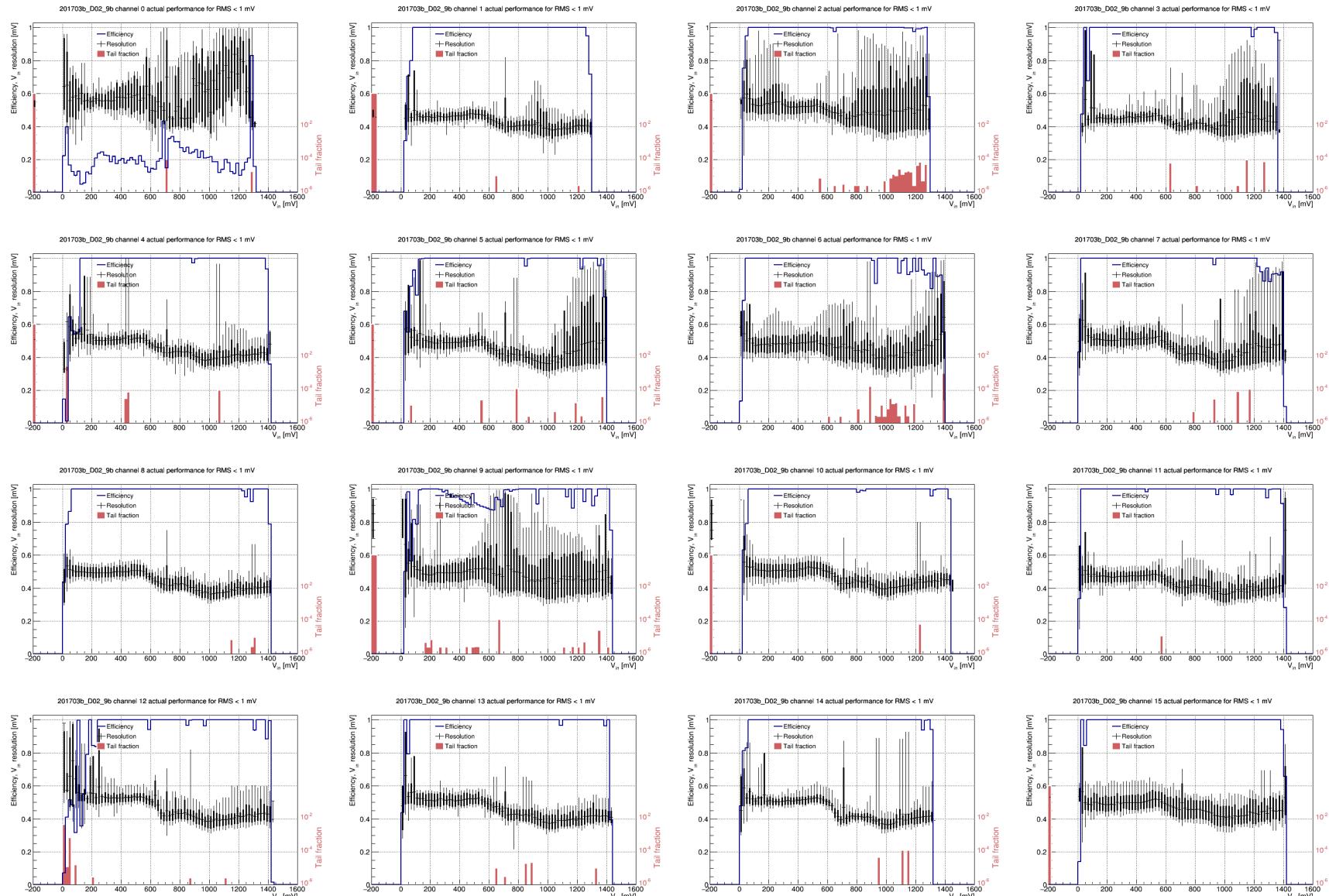
Performance: chip D02, time 8c



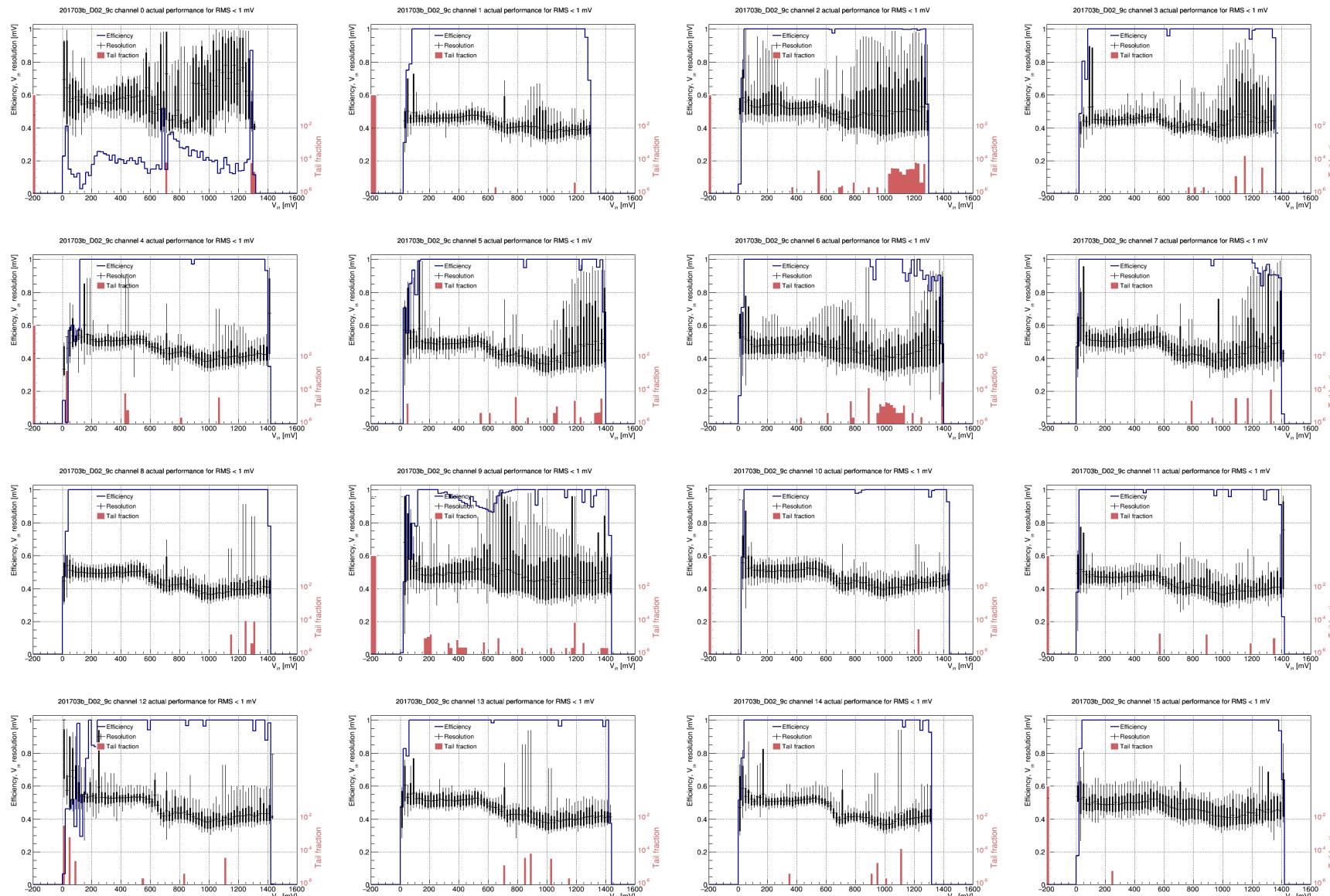
Performance: chip D02, time 9a



Performance: chip D02, time 9b

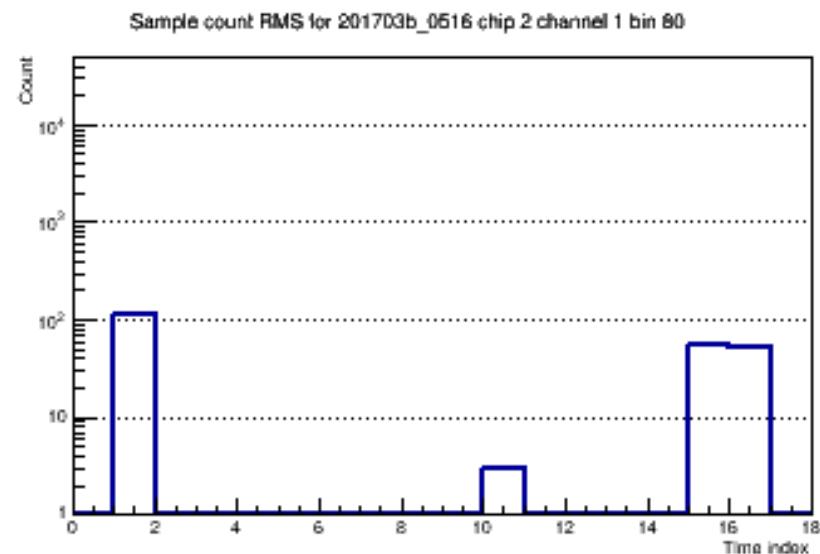
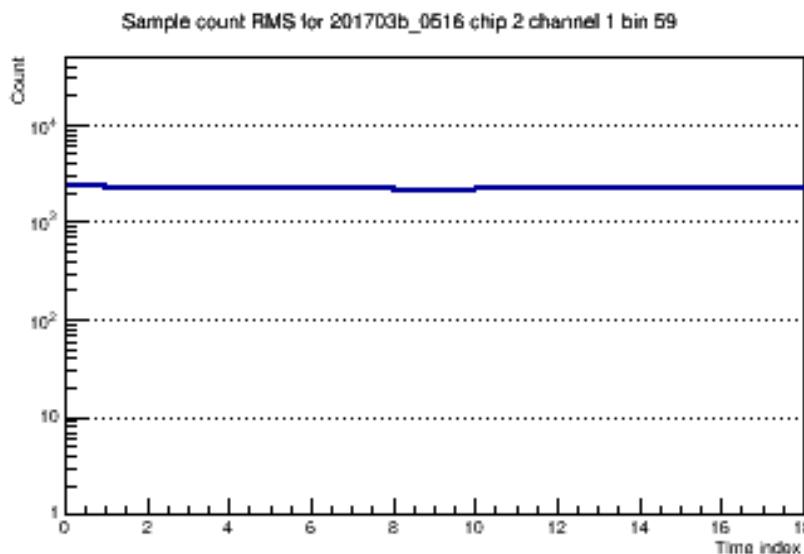
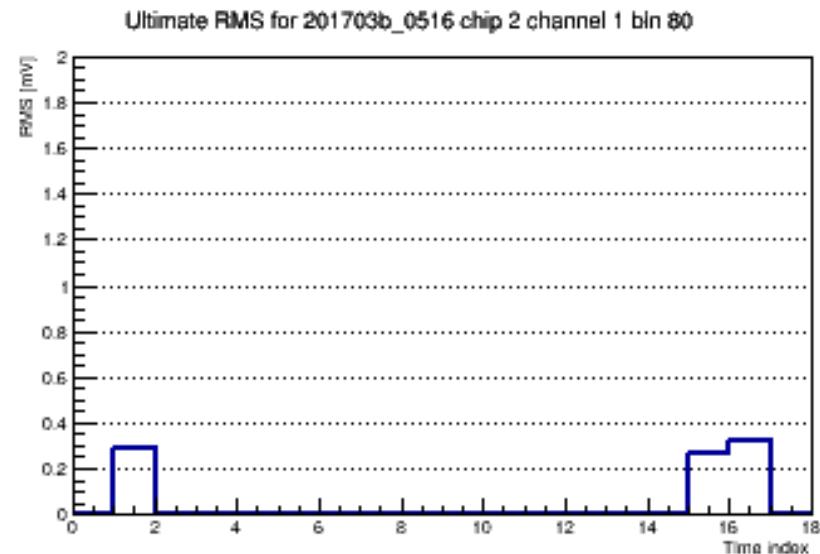
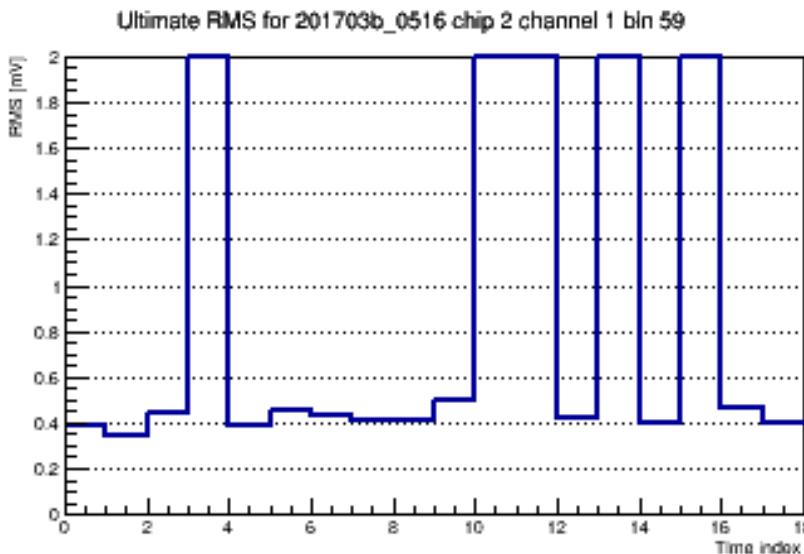


Performance: chip D02, time 9c



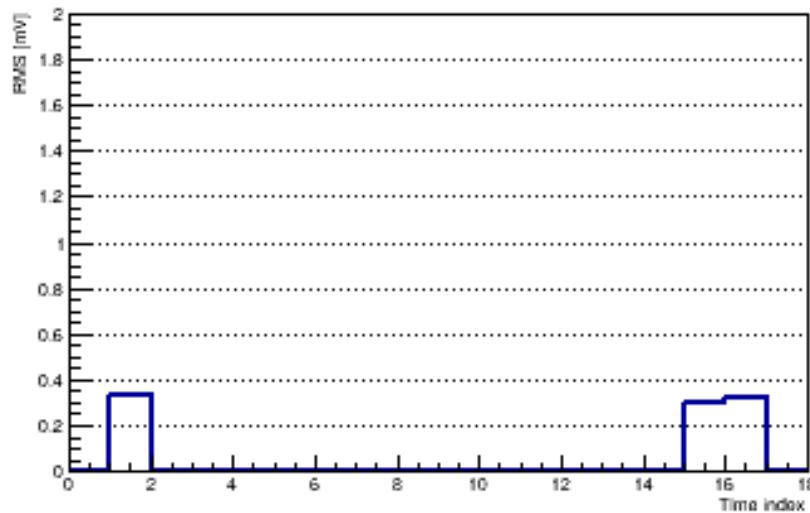
Appendix 3: Time variation

Time varying bins 1

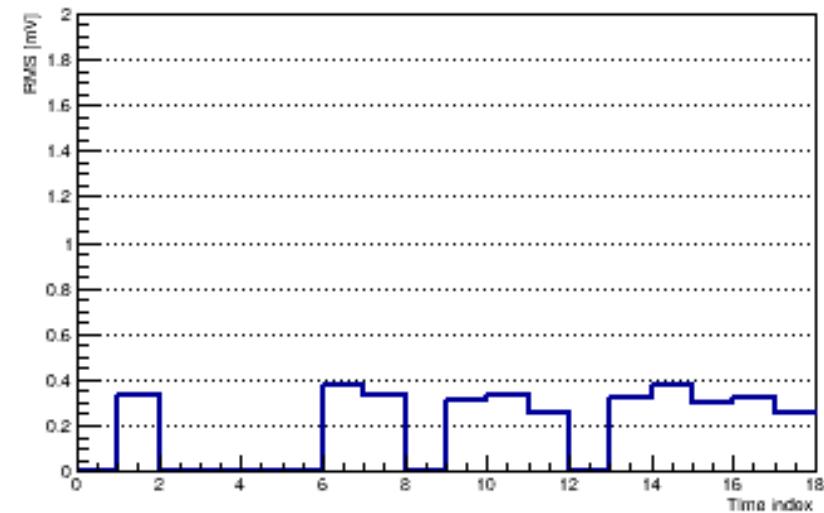


Time varying bins 2

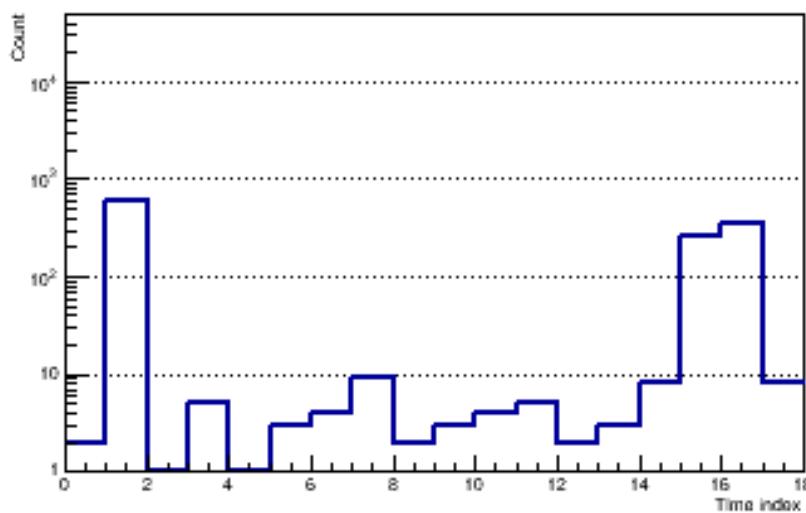
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 81



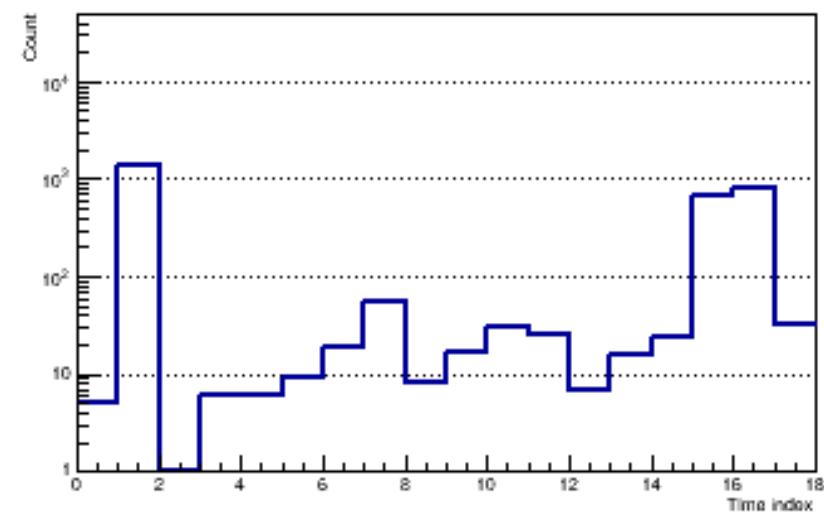
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 82



Sample count RMS for 201703b_0516 chip 2 channel 1 bin 81

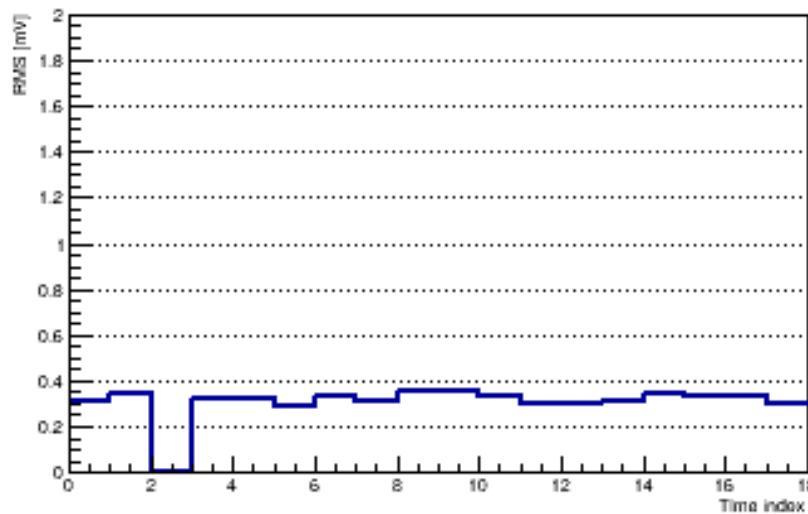


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 82

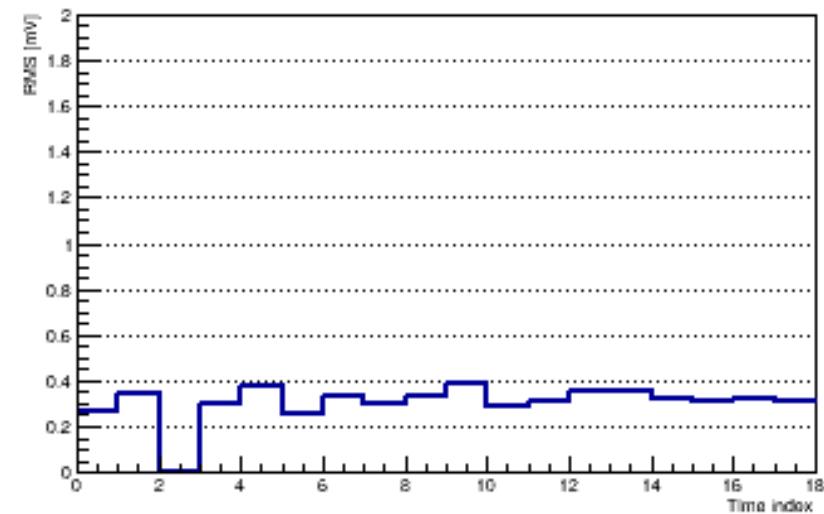


Time varying bins 3

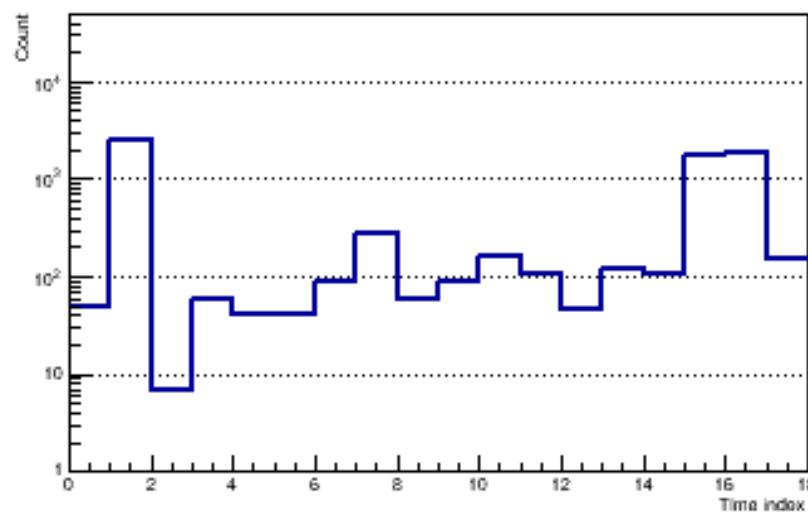
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 83



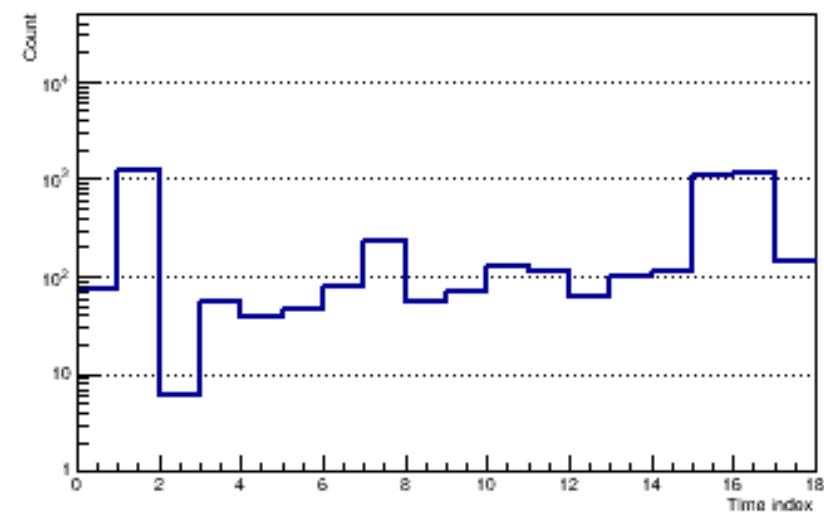
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 84



Sample count RMS for 201703b_0516 chip 2 channel 1 bin 83

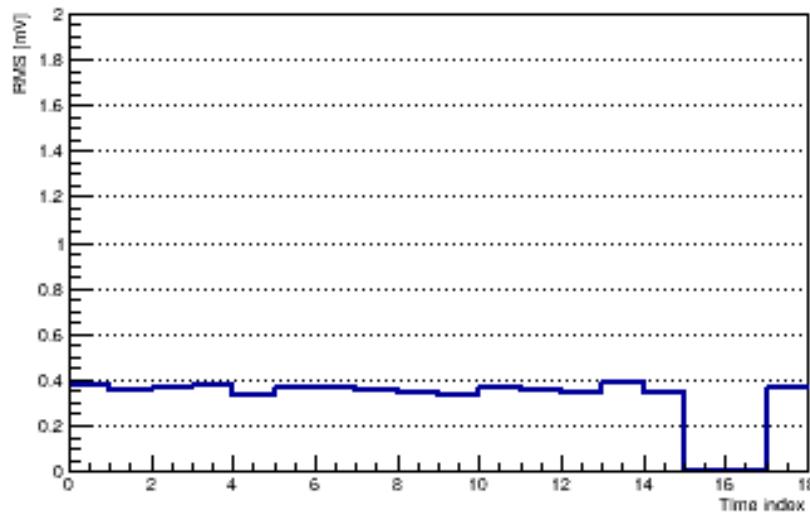


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 84

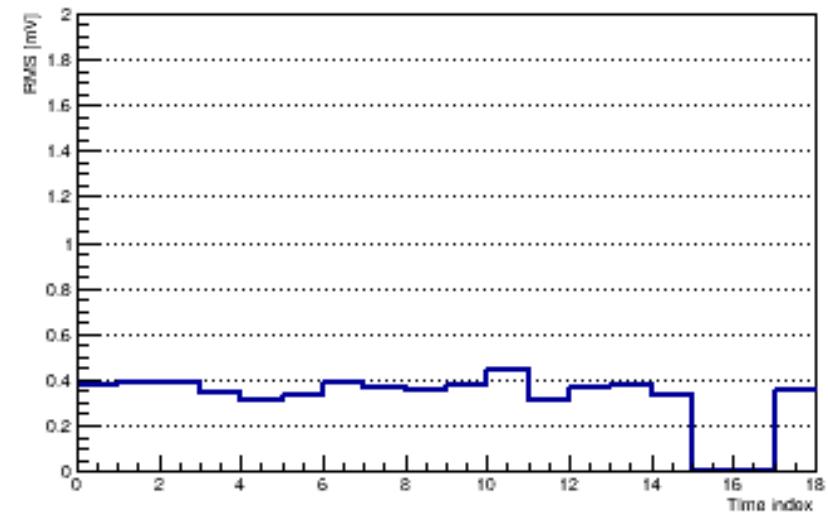


Time varying bins 4

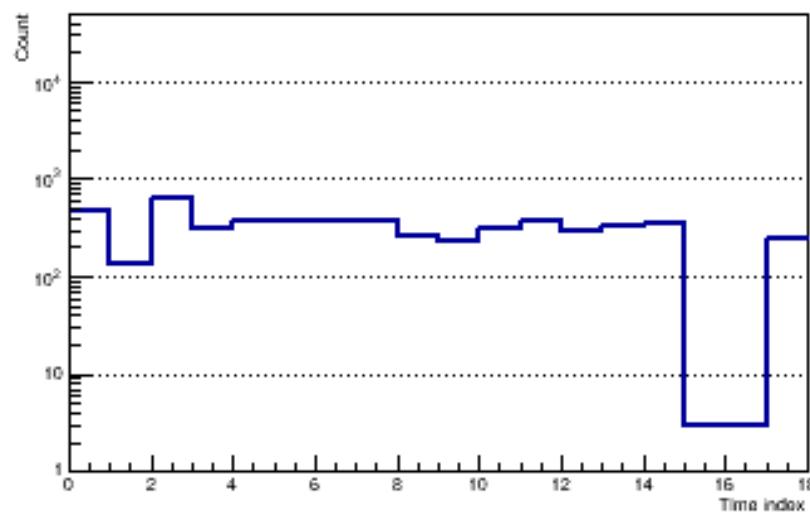
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 109



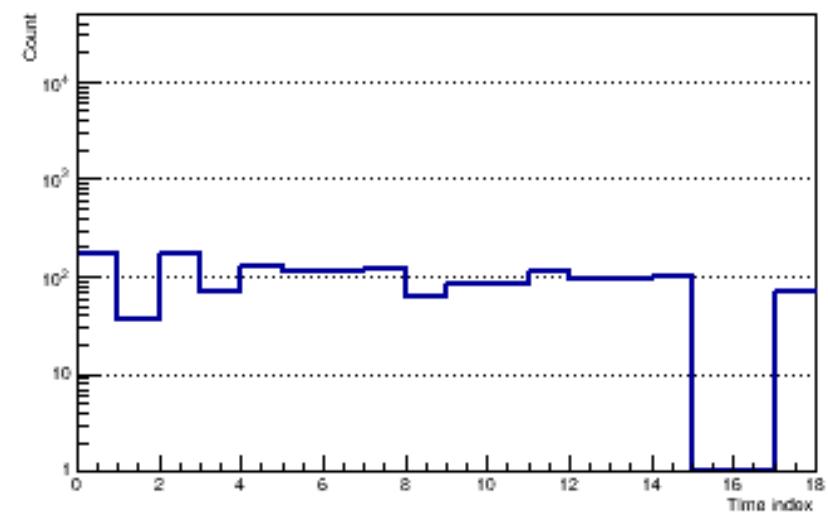
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 110



Sample count RMS for 201703b_0516 chip 2 channel 1 bin 109

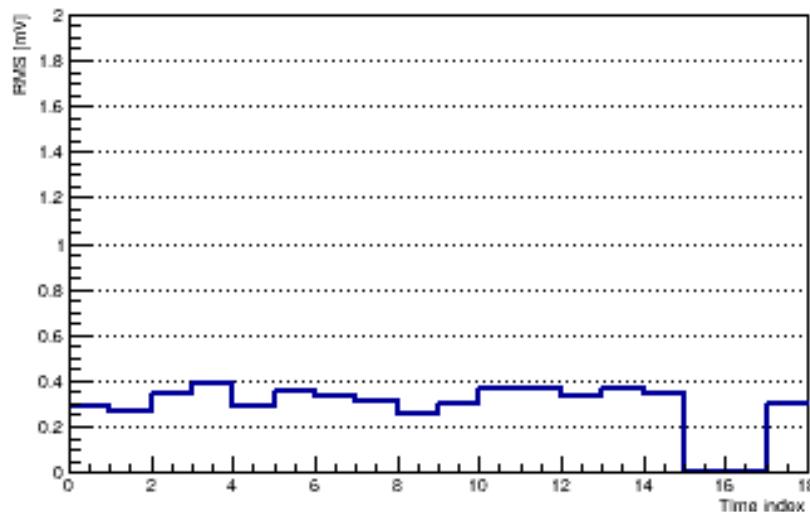


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 110

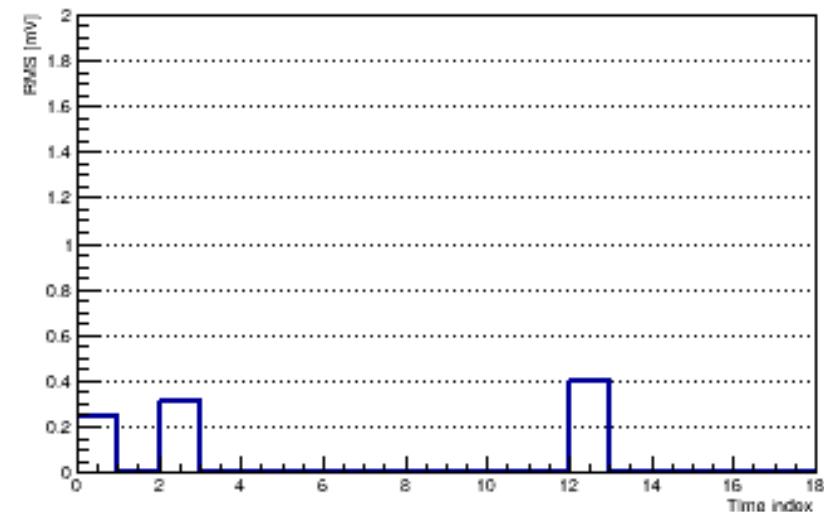


Time varying bins 5

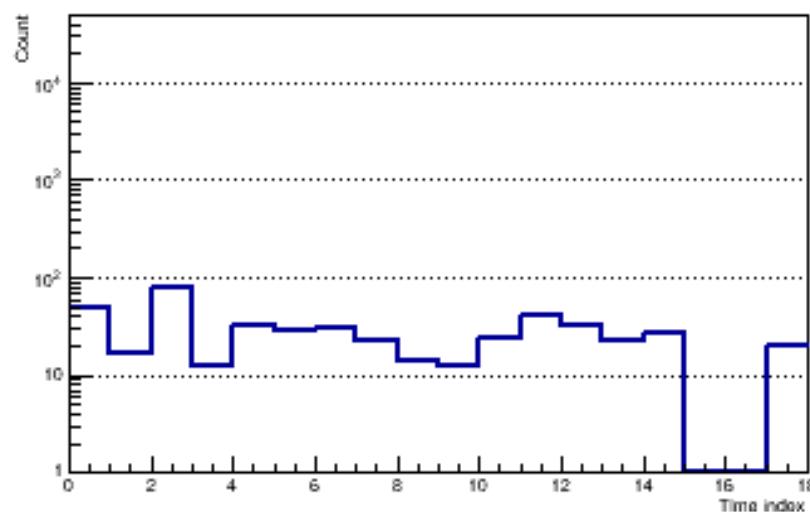
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 111



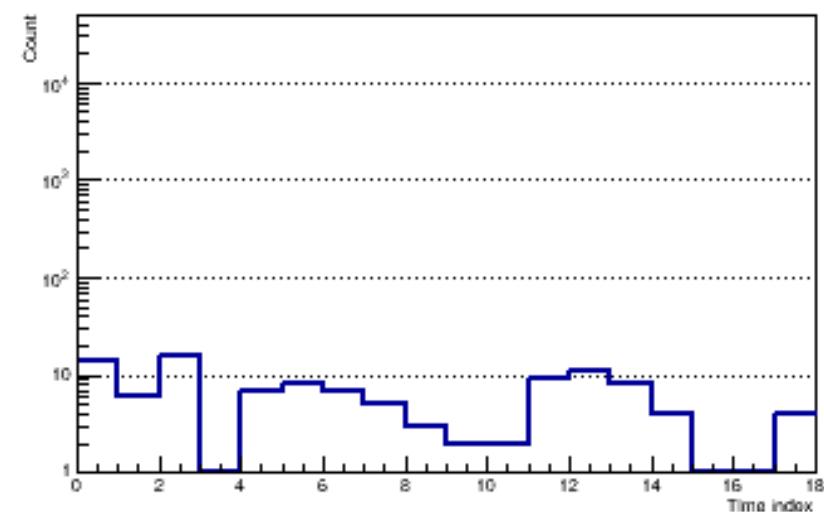
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 112



Sample count RMS for 201703b_0516 chip 2 channel 1 bin 111

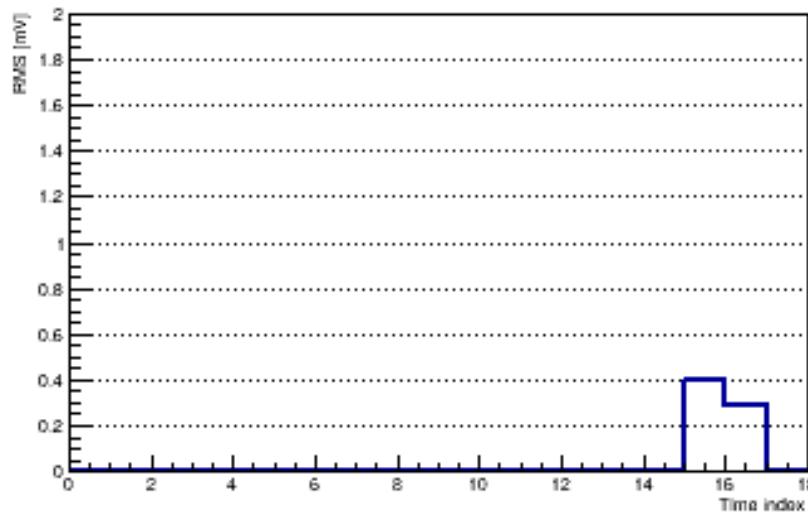


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 112

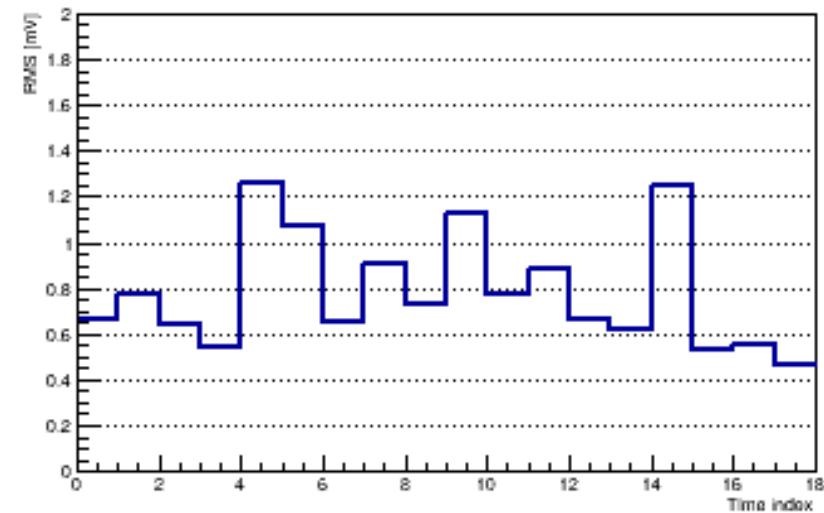


Time varying bins 6

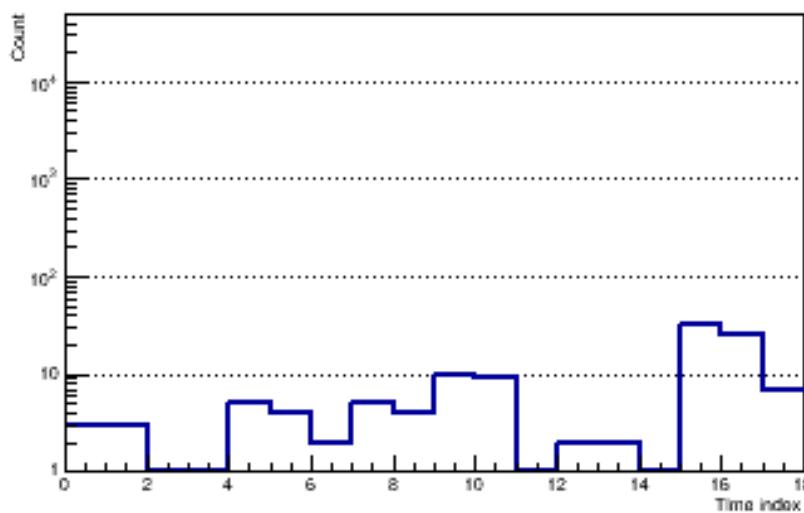
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 199



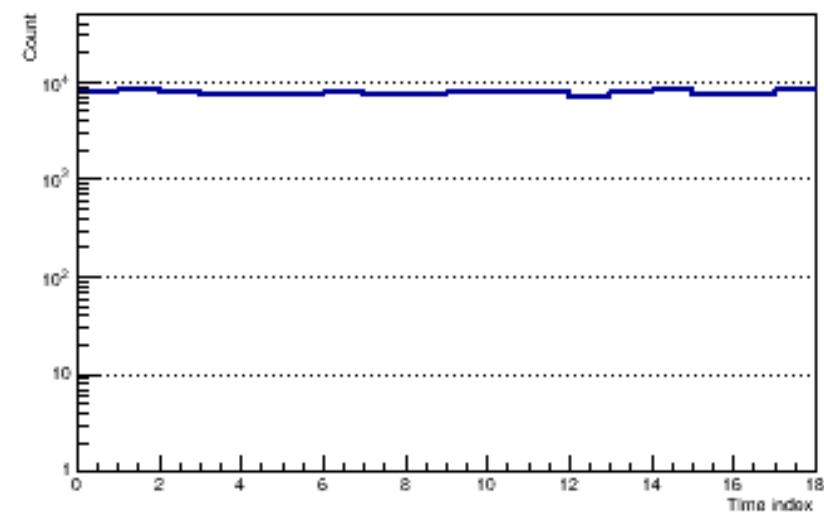
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 1983



Sample count RMS for 201703b_0516 chip 2 channel 1 bin 199

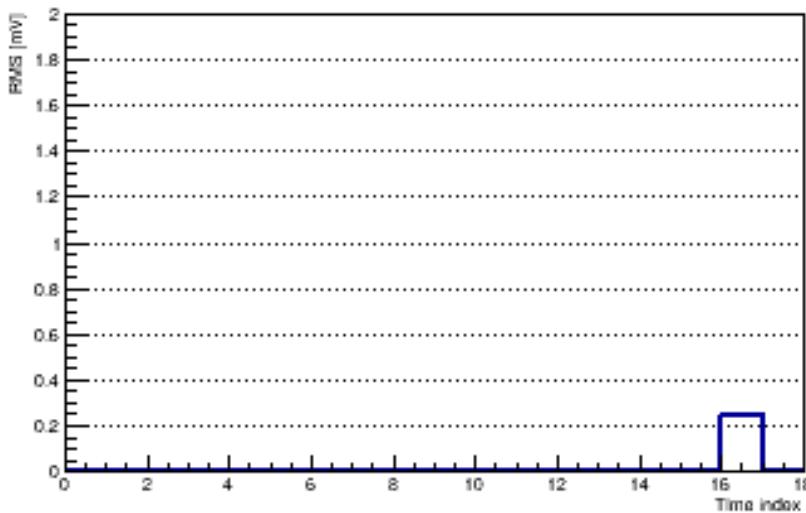


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 1983

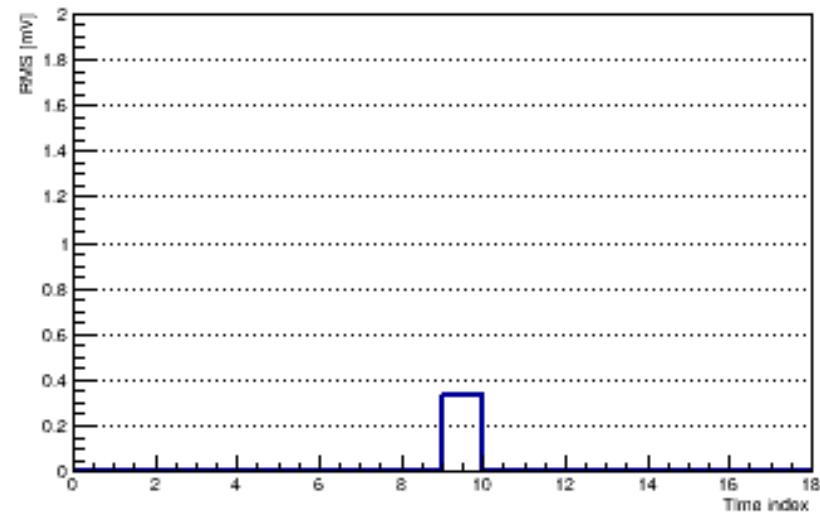


Time varying bins 7

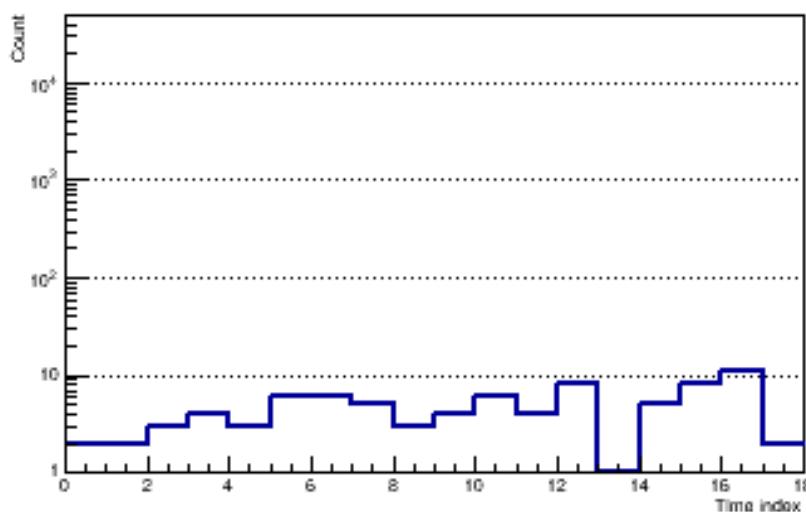
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 3072



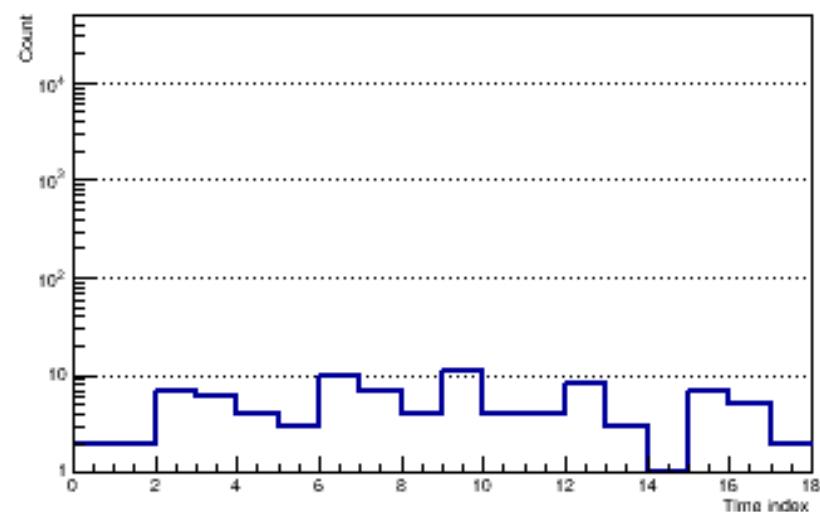
Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 3136



Sample count RMS for 201703b_0516 chip 2 channel 1 bin 3072

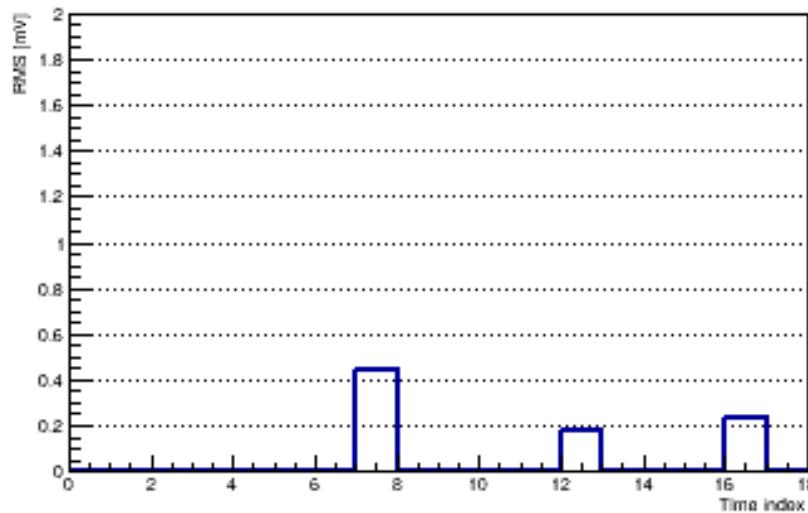


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 3136

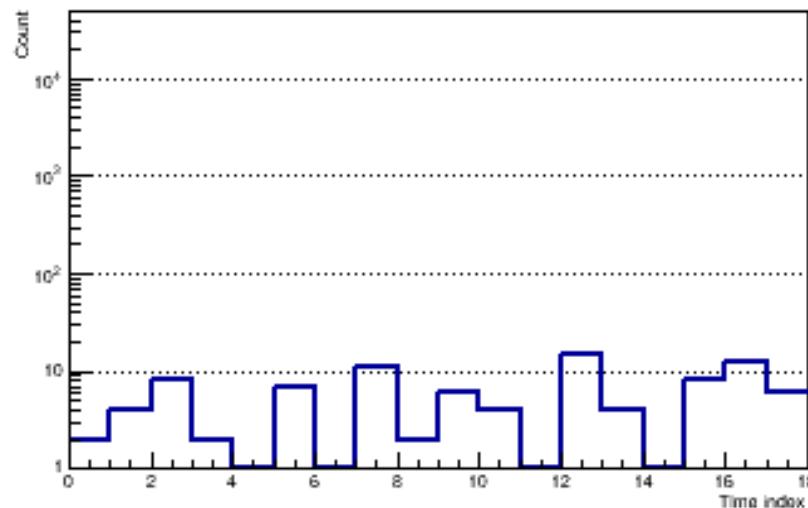


Time varying bins 8

Ultimate RMS for 201703b_0516 chip 2 channel 1 bin 3328

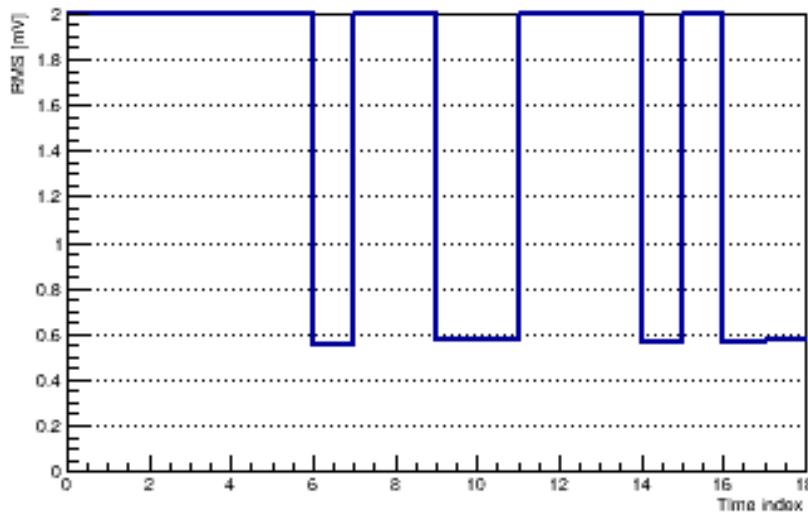


Sample count RMS for 201703b_0516 chip 2 channel 1 bin 3328

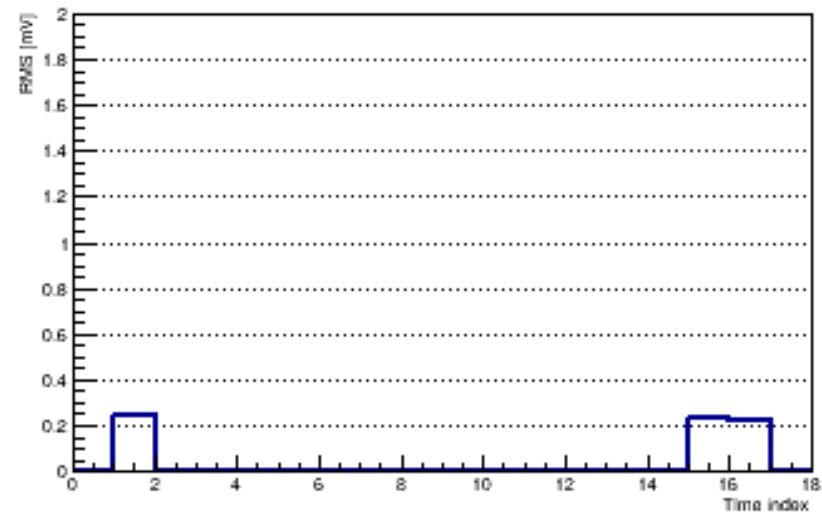


Time varying bins 9

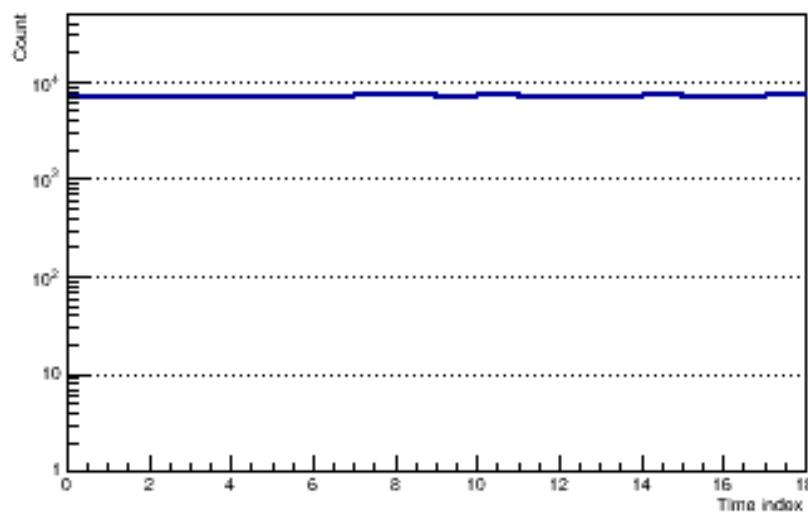
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 46



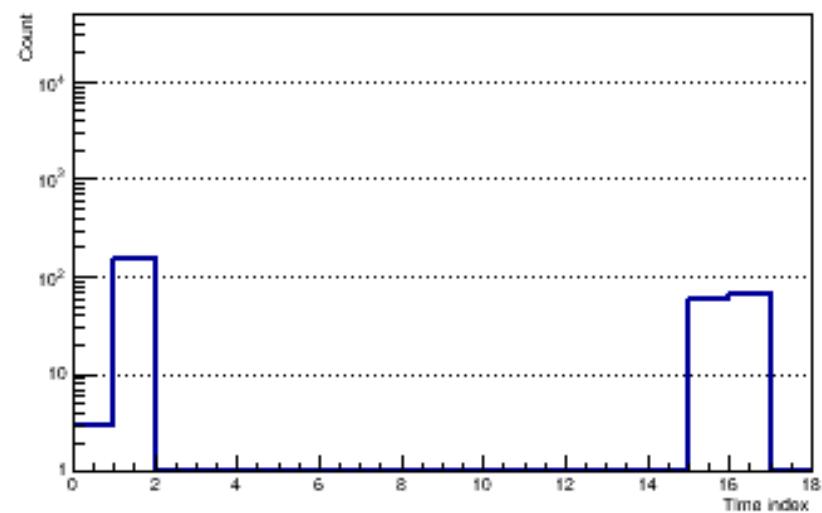
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 64



Sample count RMS for 201703b_0516 chip 2 channel 2 bin 46

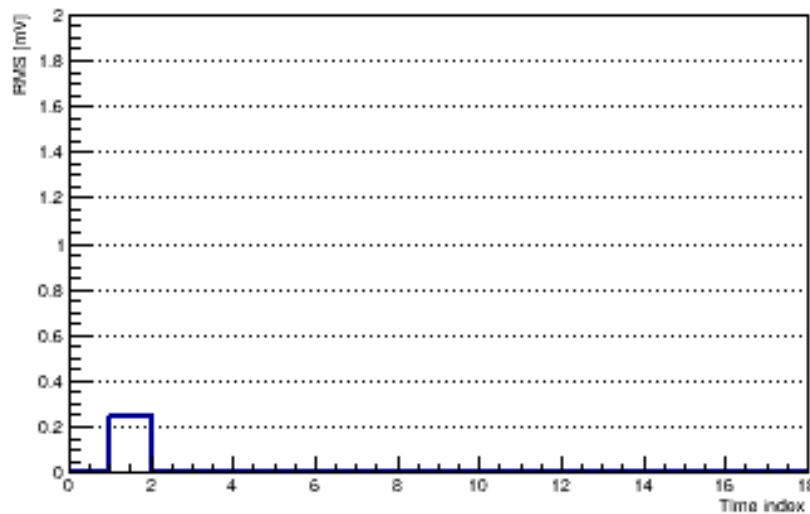


Sample count RMS for 201703b_0516 chip 2 channel 2 bin 64

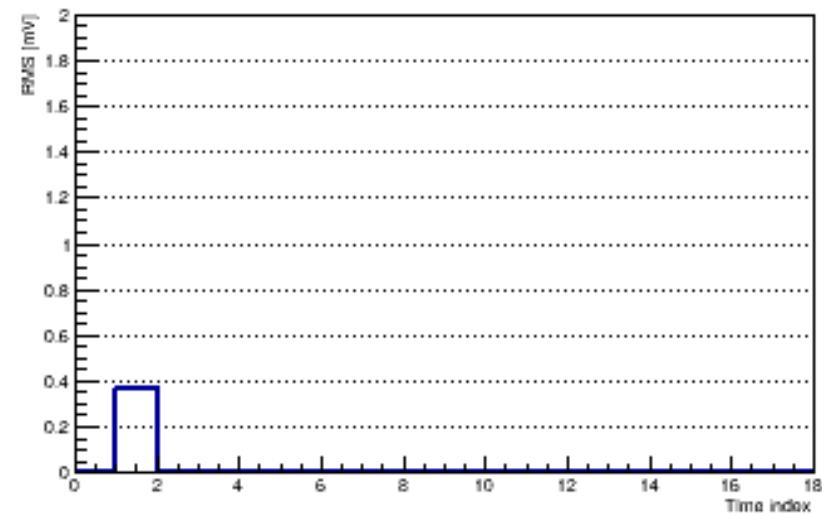


Time varying bins 10

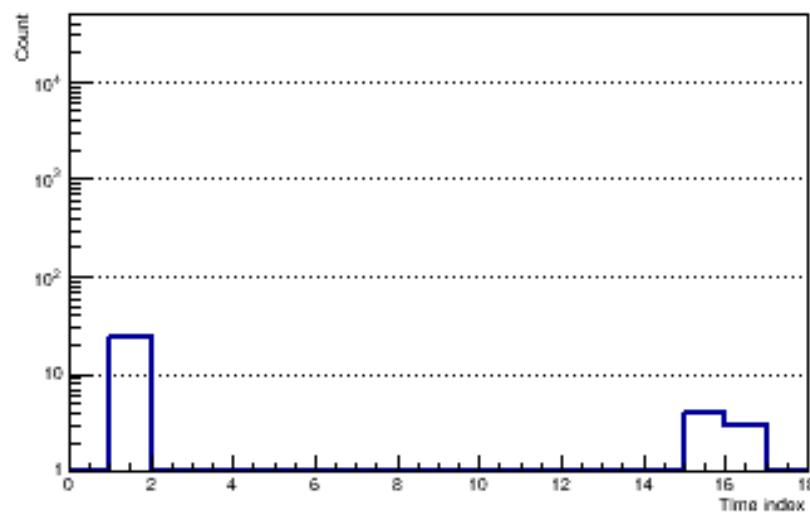
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 69



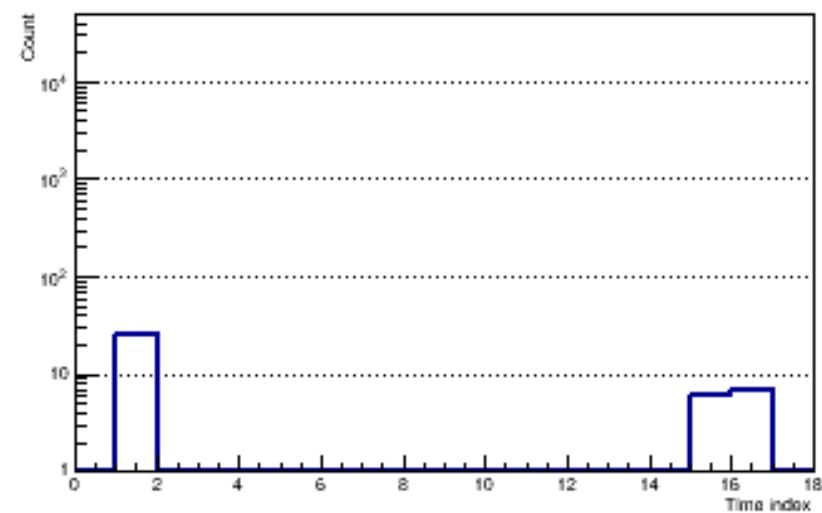
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 70



Sample count RMS for 201703b_0516 chip 2 channel 2 bin 69

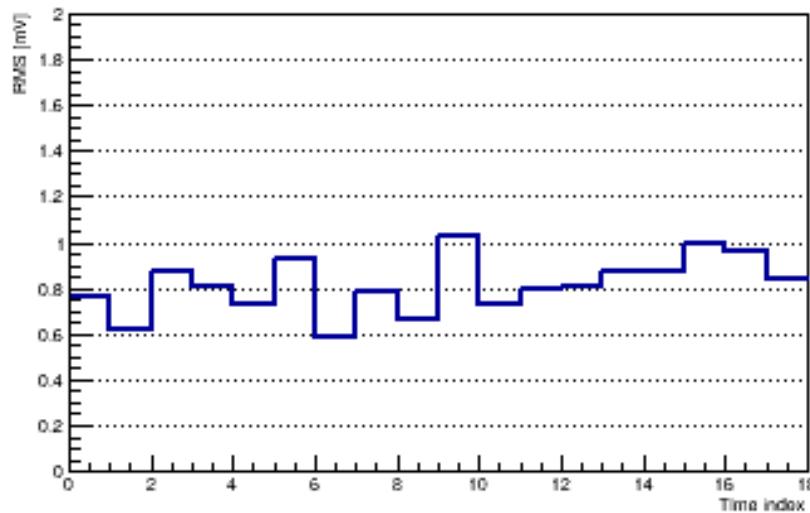


Sample count RMS for 201703b_0516 chip 2 channel 2 bin 70

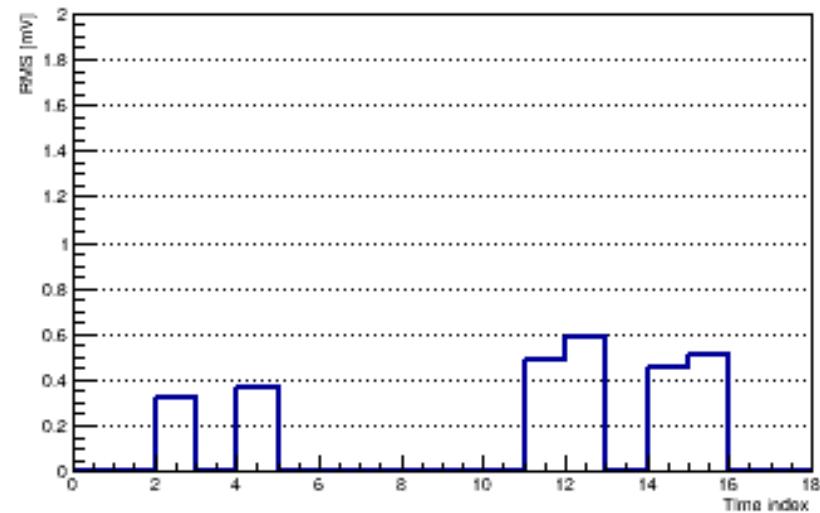


Time varying bins 11

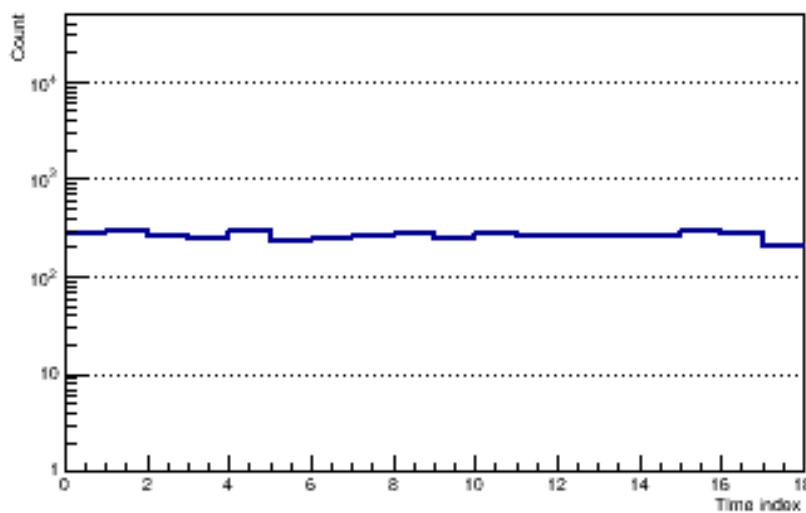
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2136



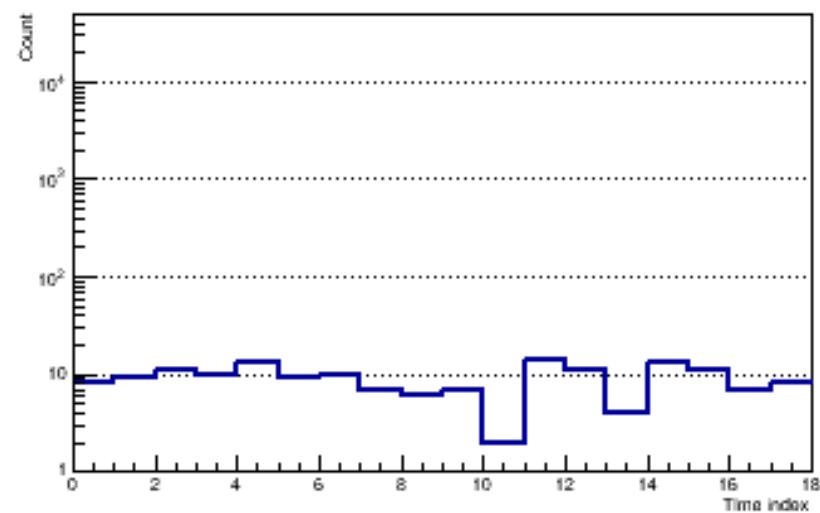
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2137



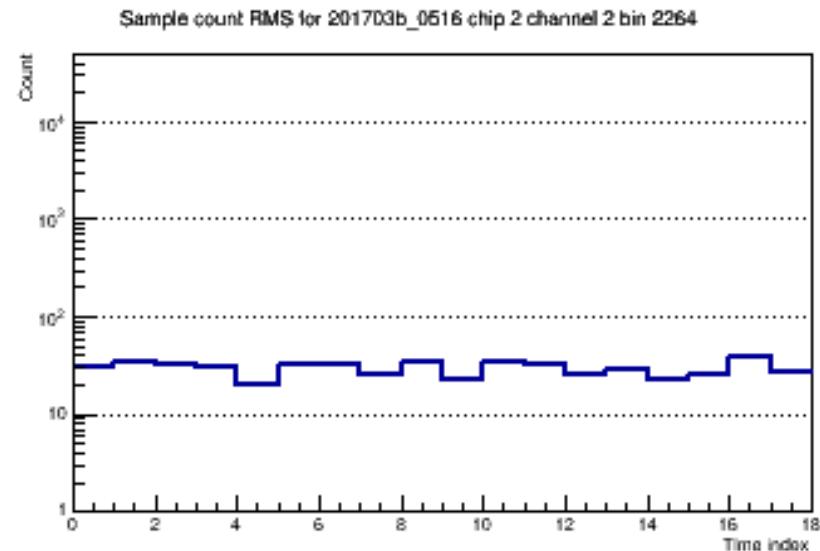
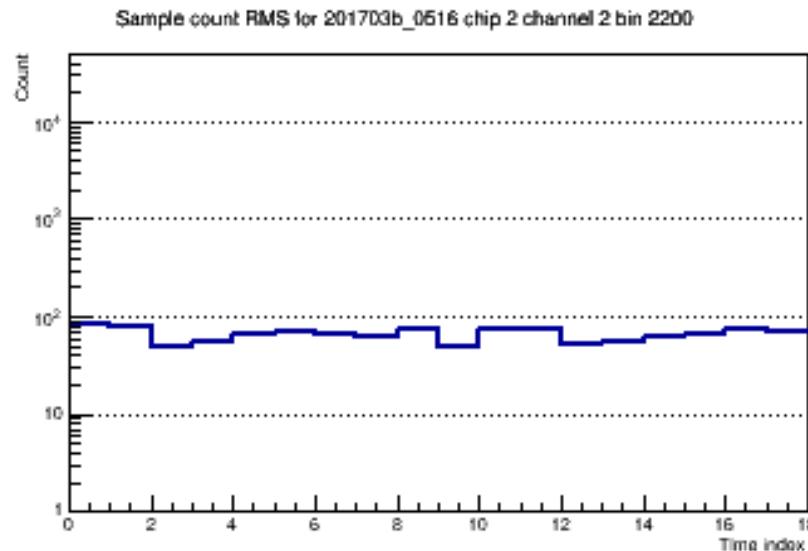
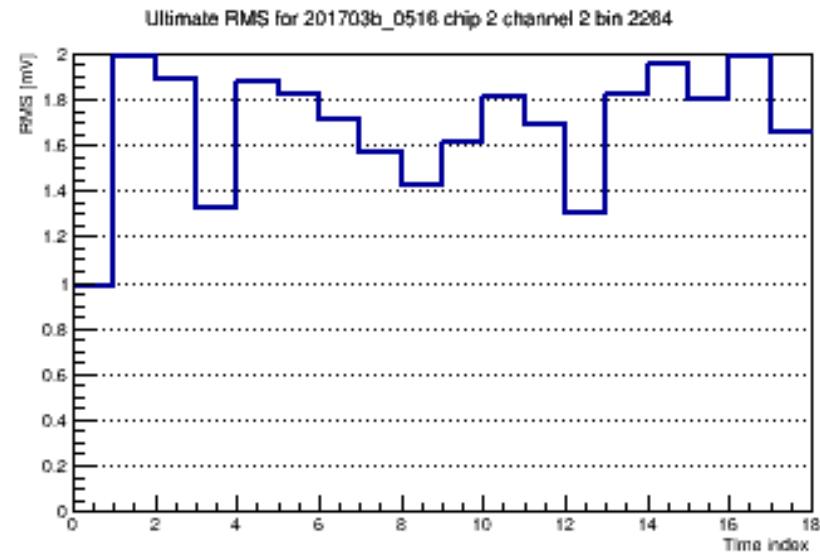
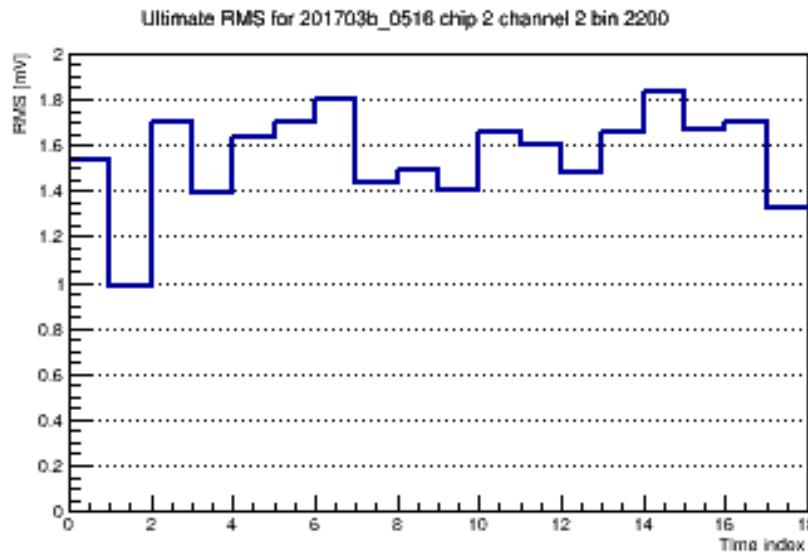
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2136



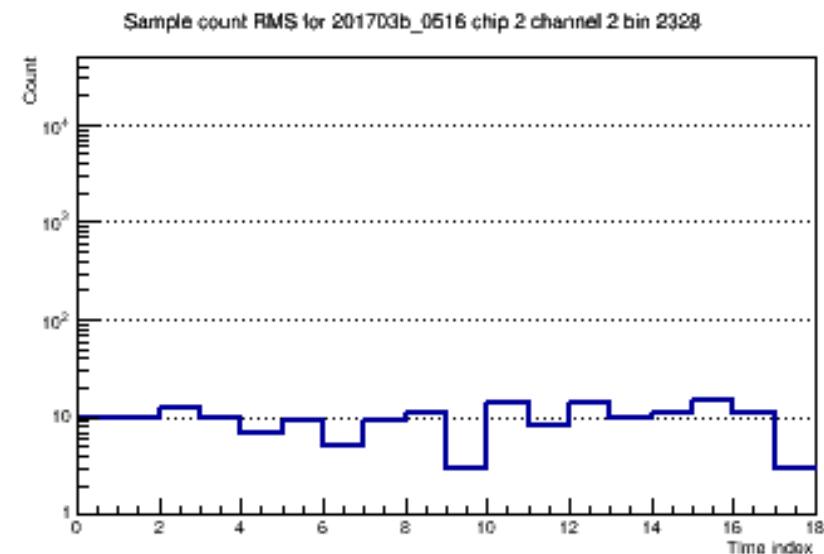
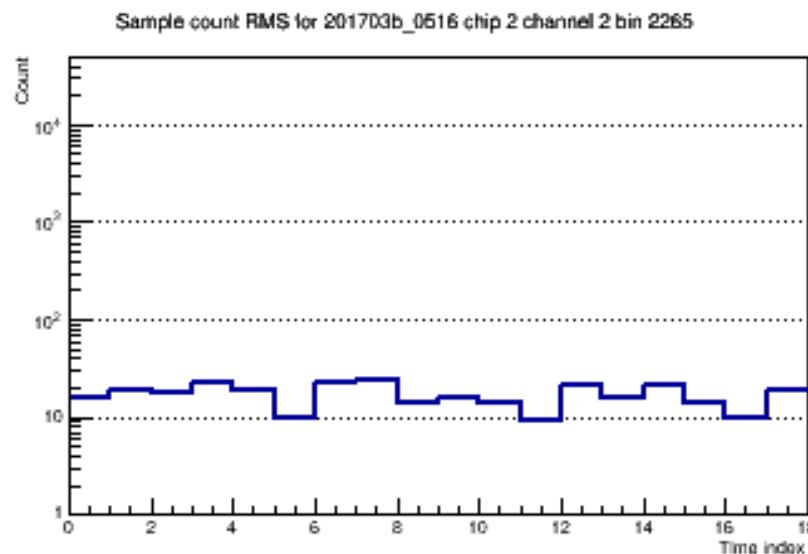
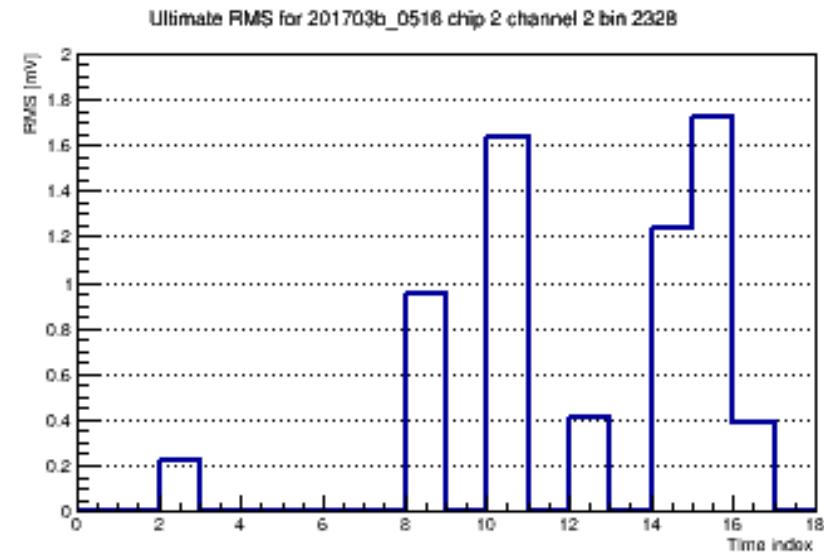
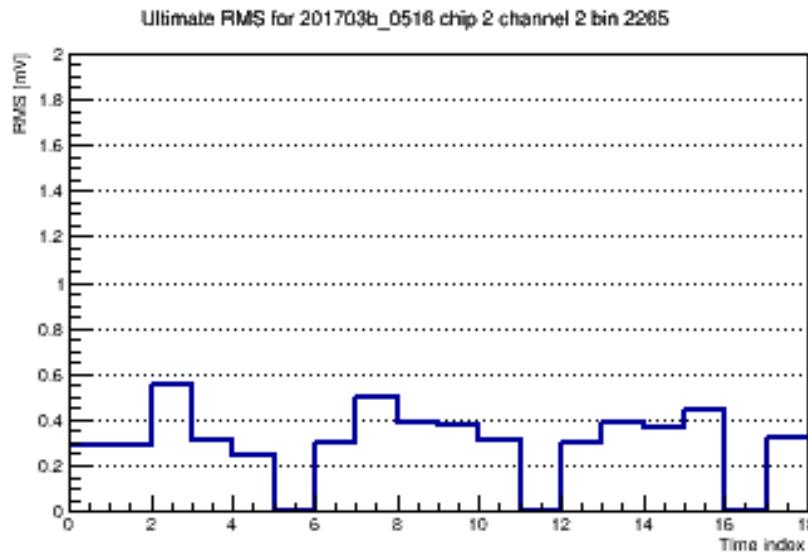
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2137



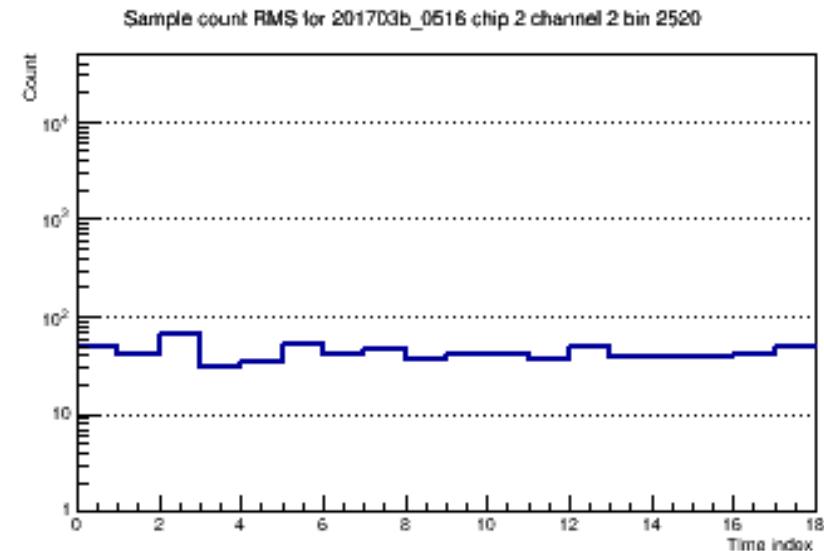
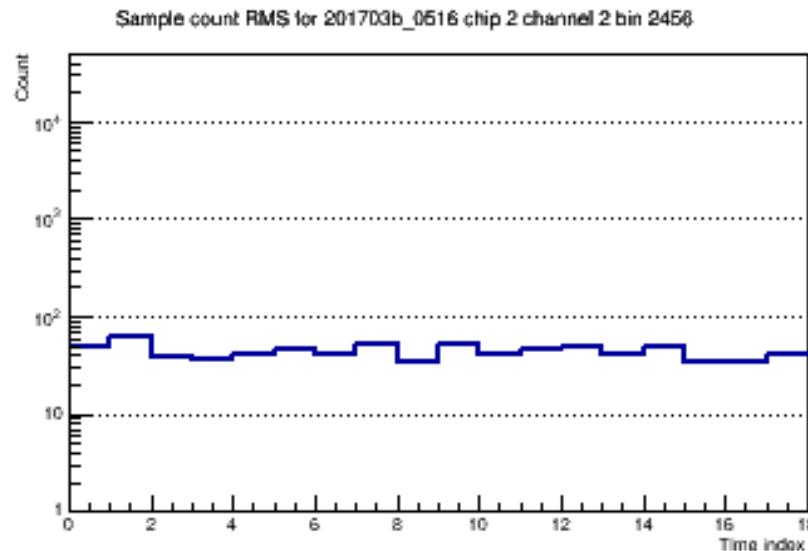
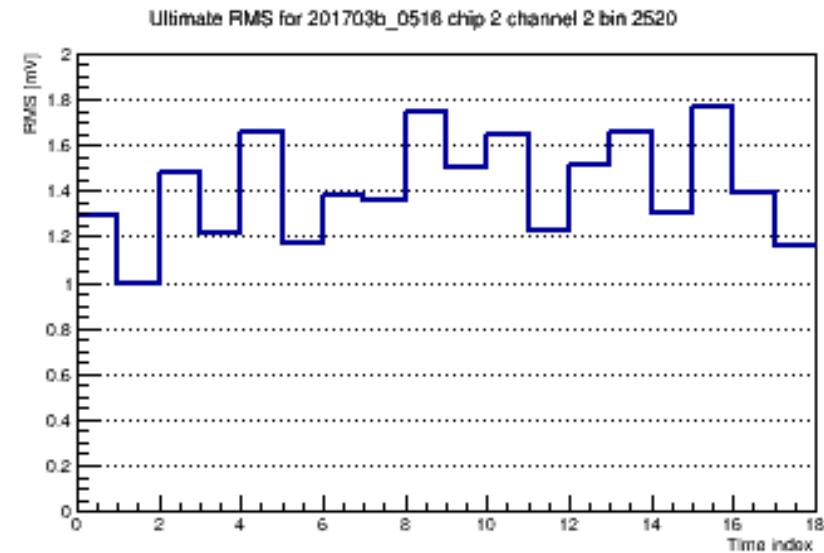
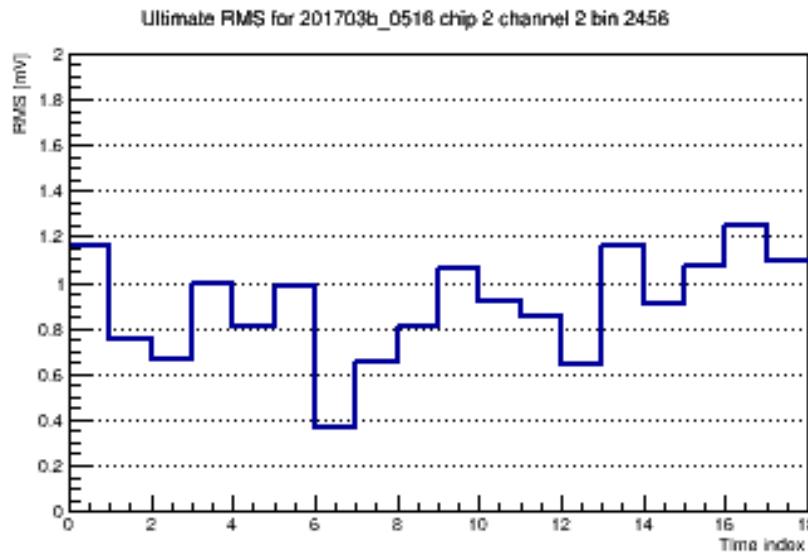
Time varying bins 12



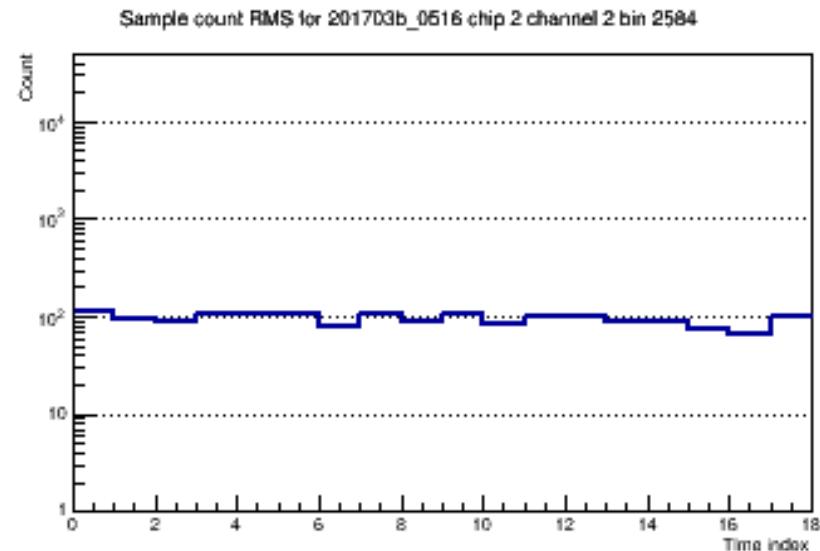
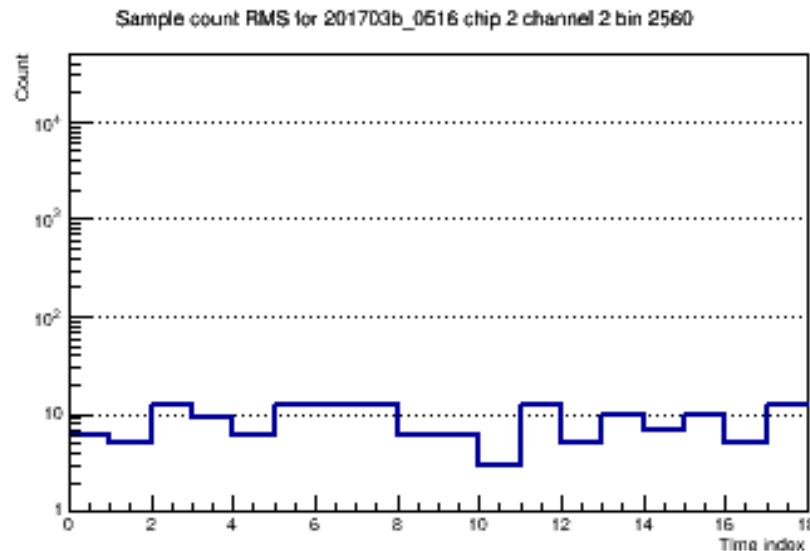
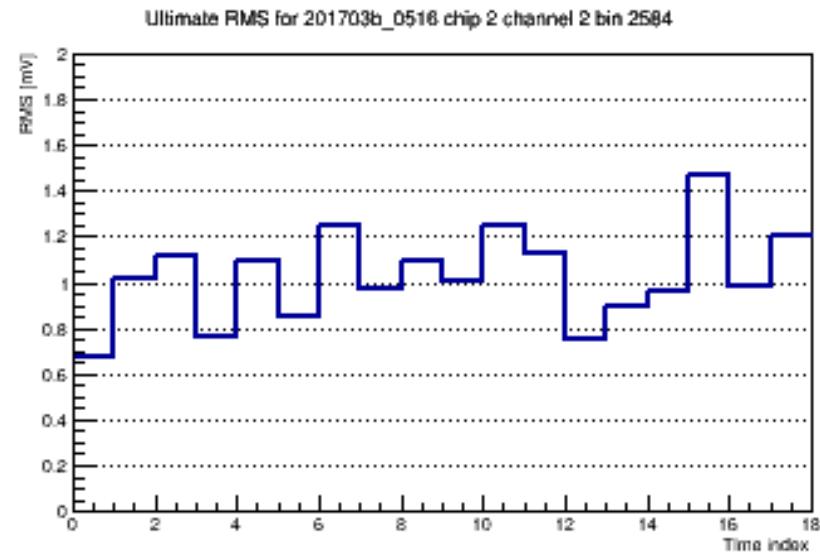
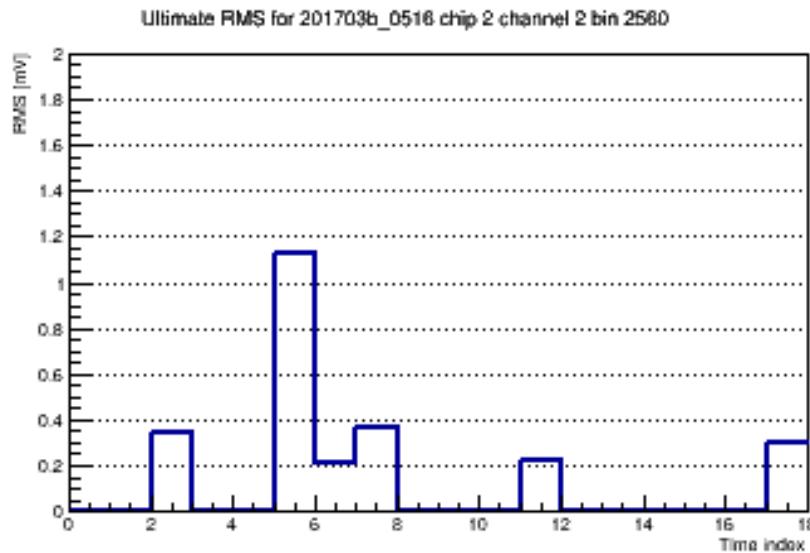
Time varying bins 13



Time varying bins 14

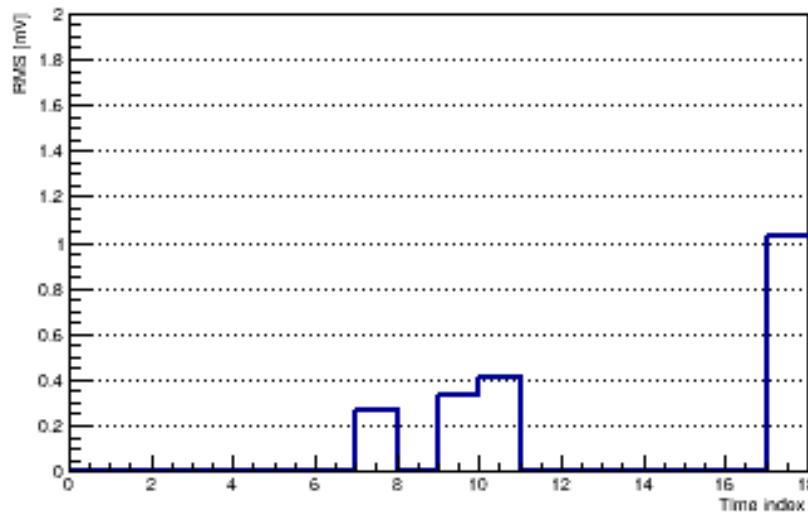


Time varying bins 15

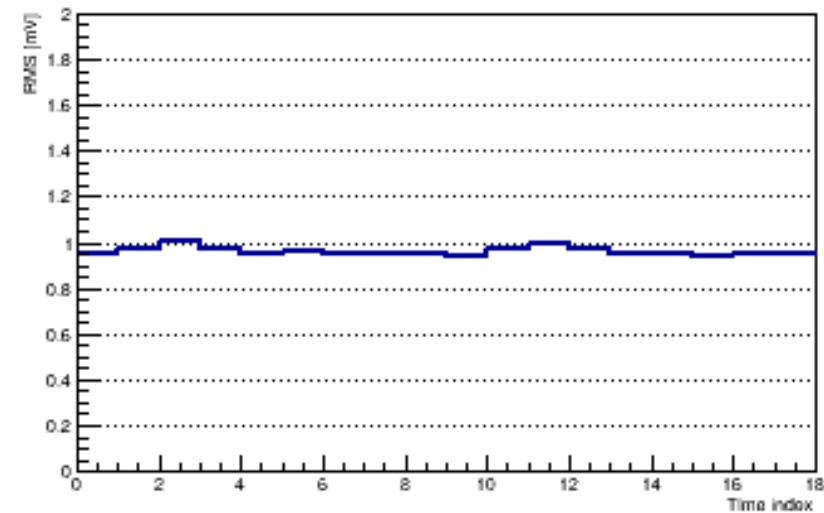


Time varying bins 16

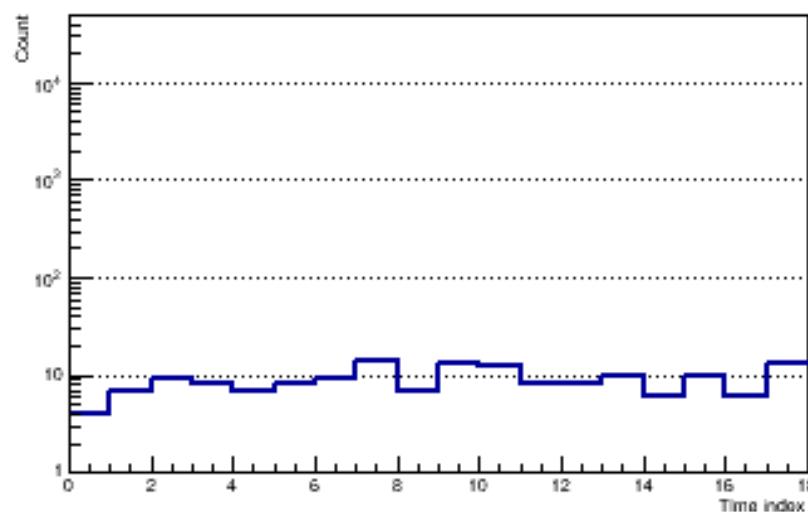
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2624



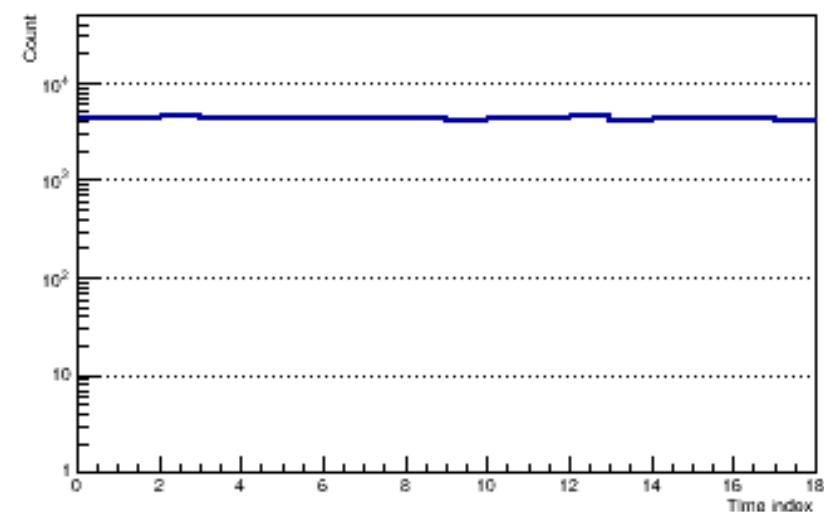
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2703



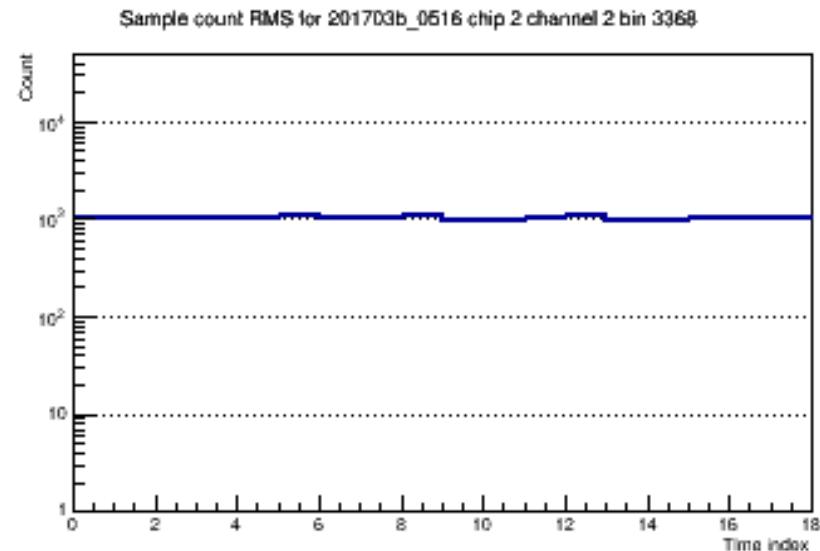
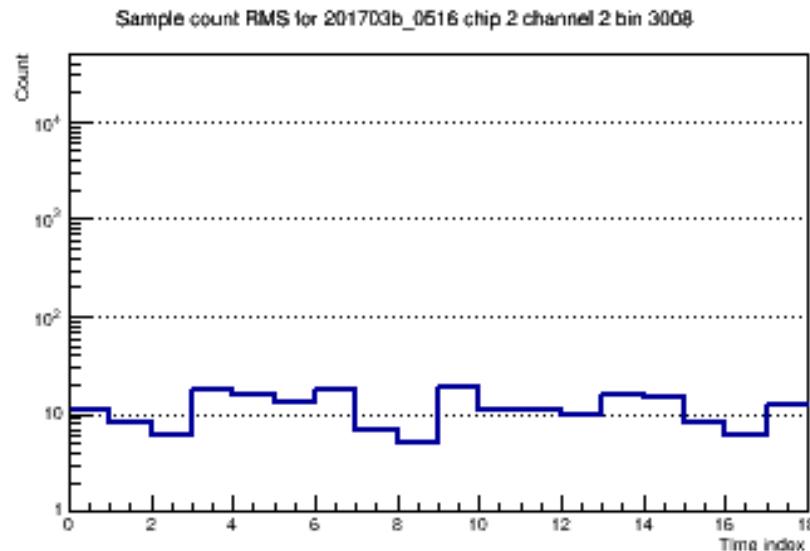
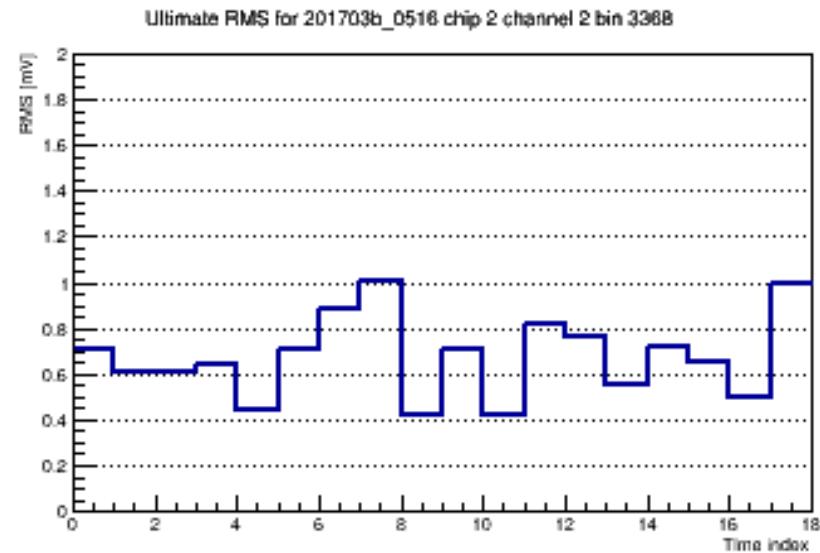
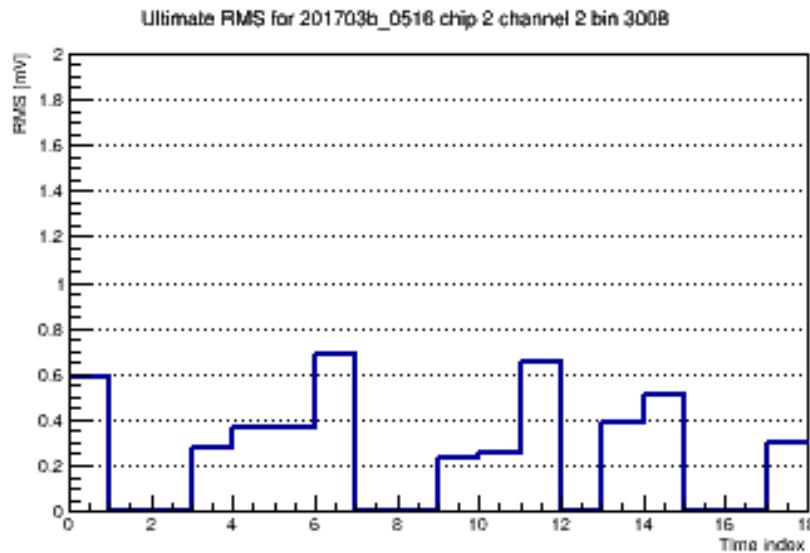
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2624



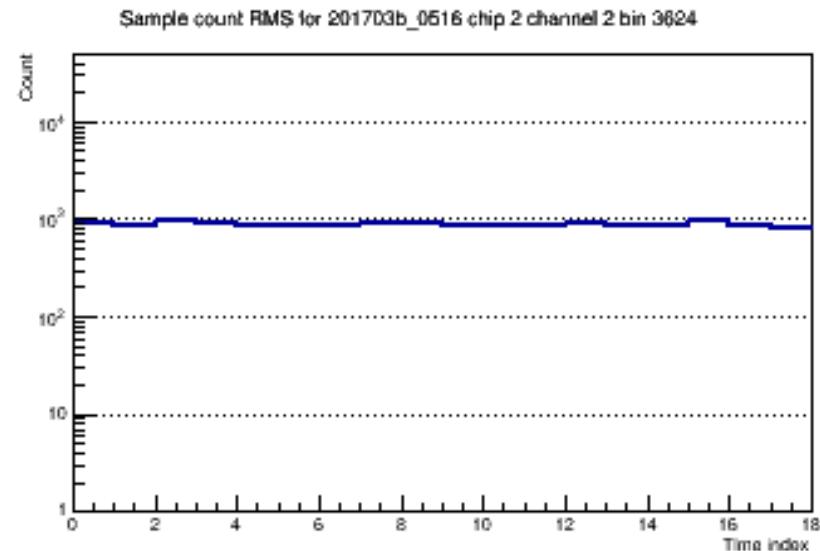
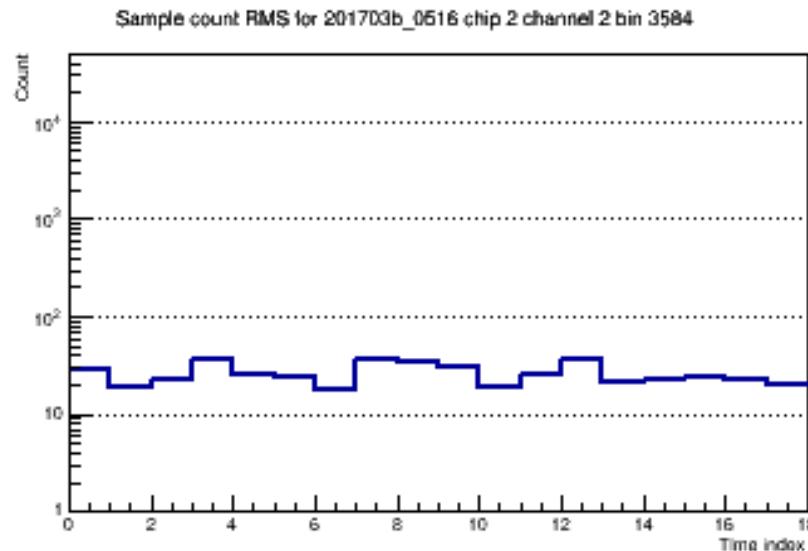
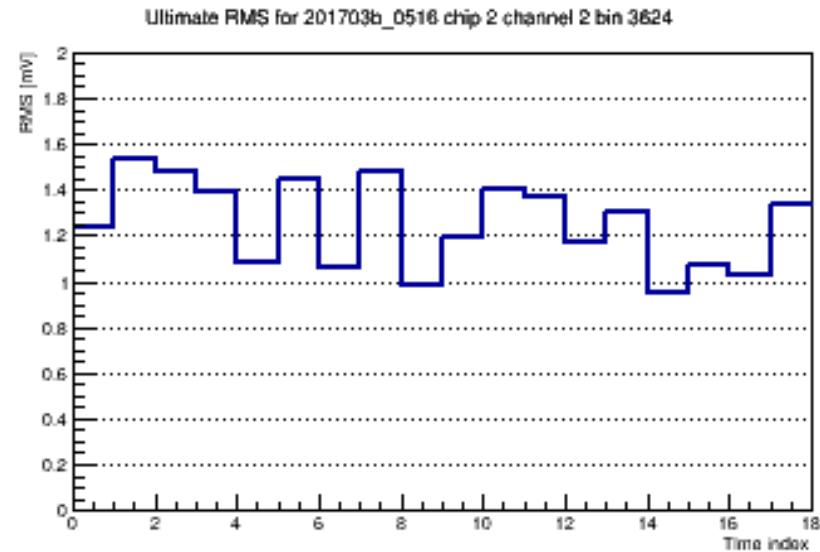
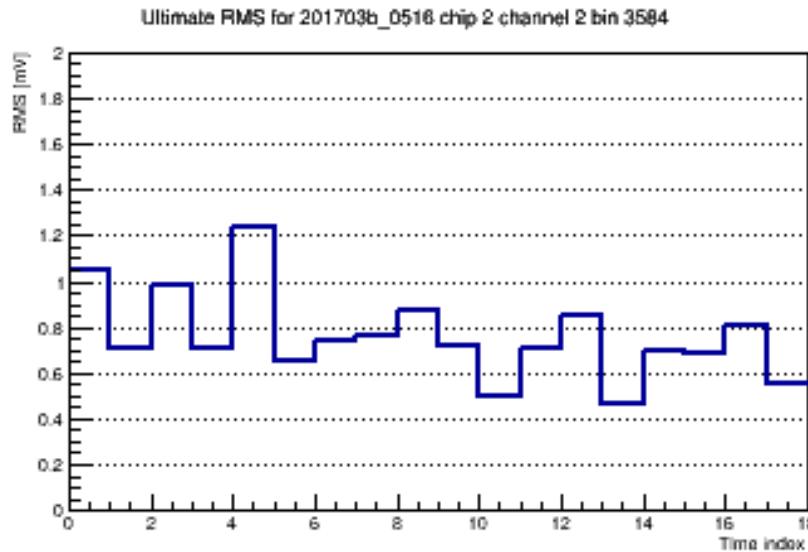
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2703



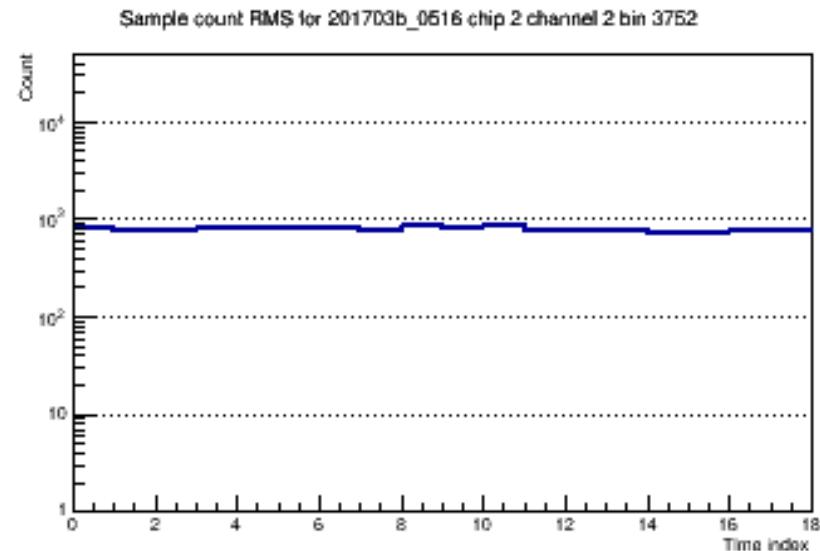
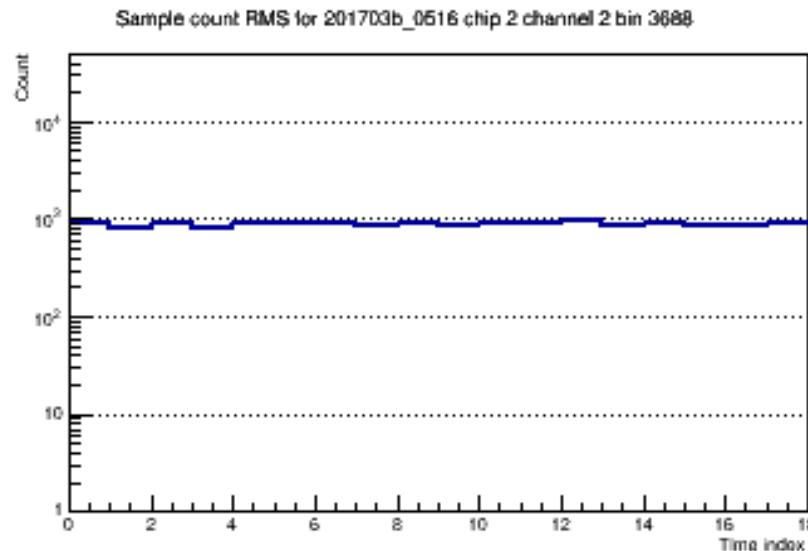
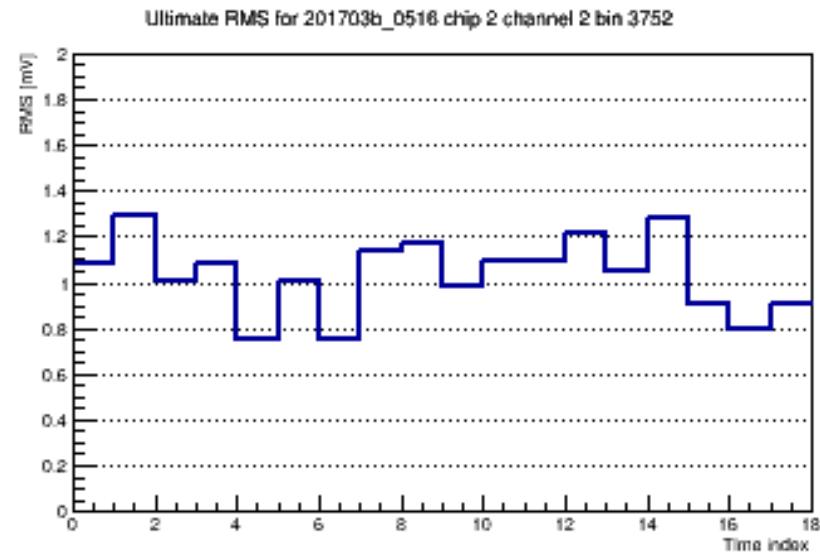
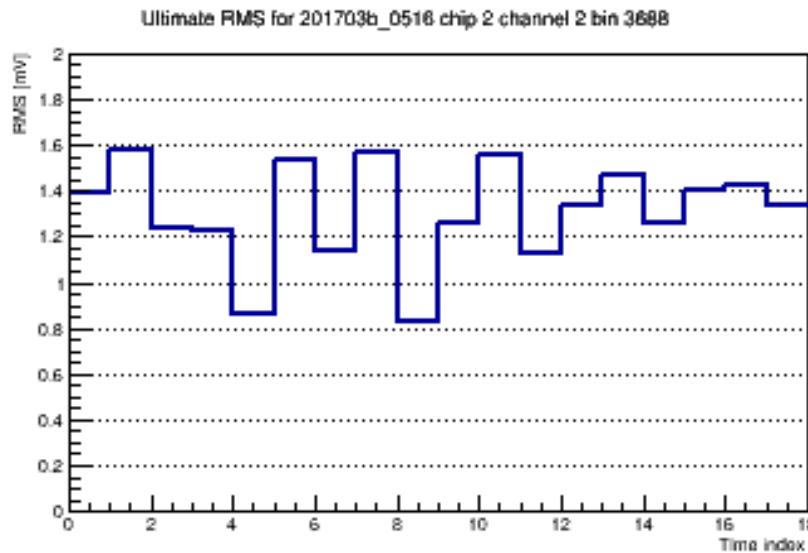
Time varying bins 17



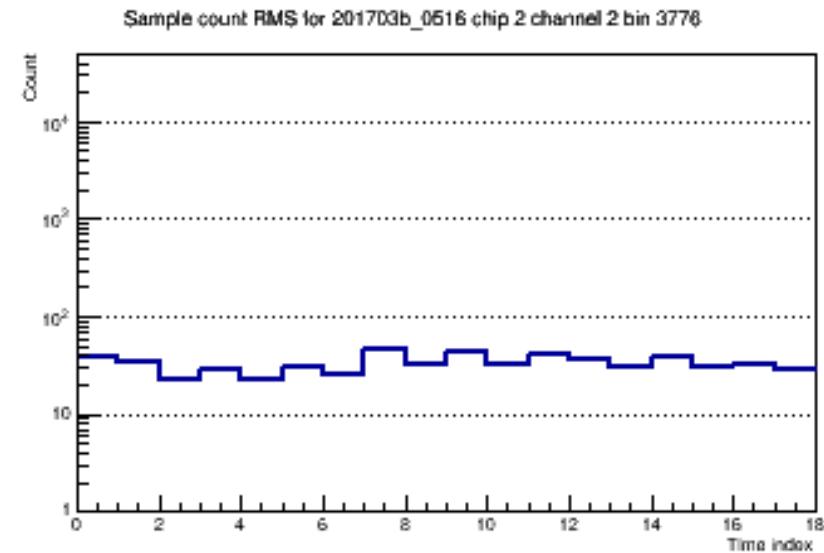
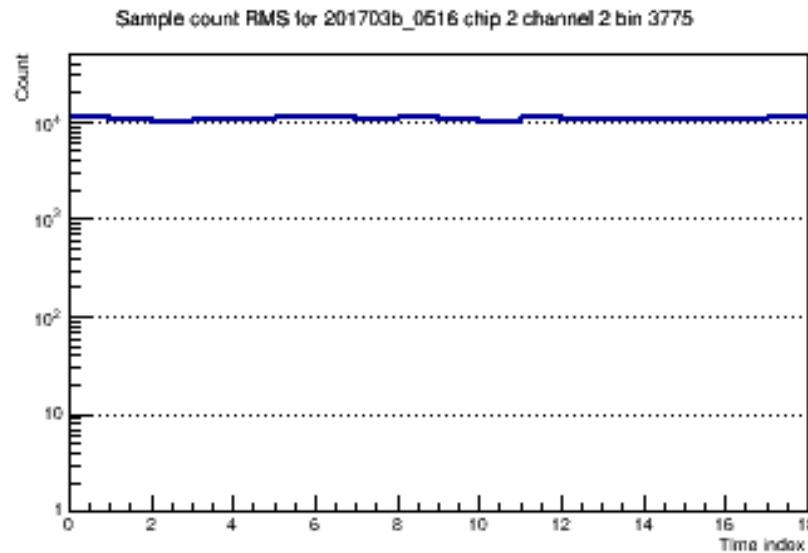
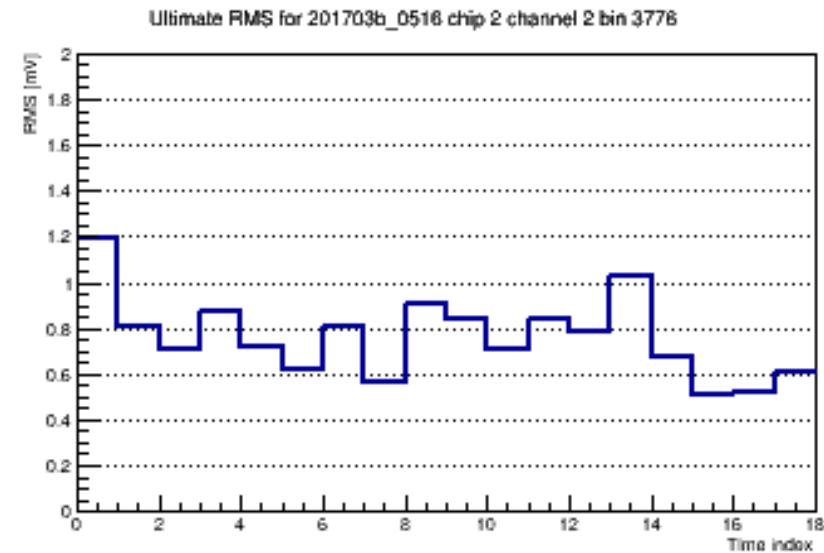
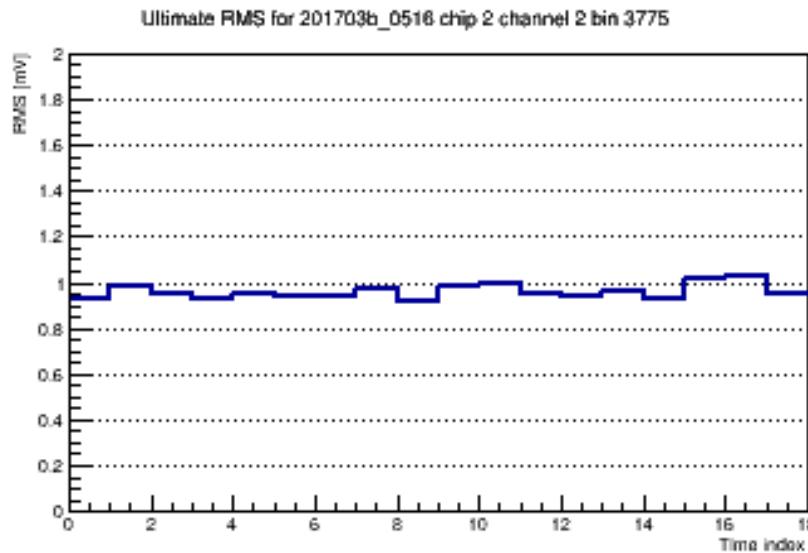
Time varying bins 18



Time varying bins 19

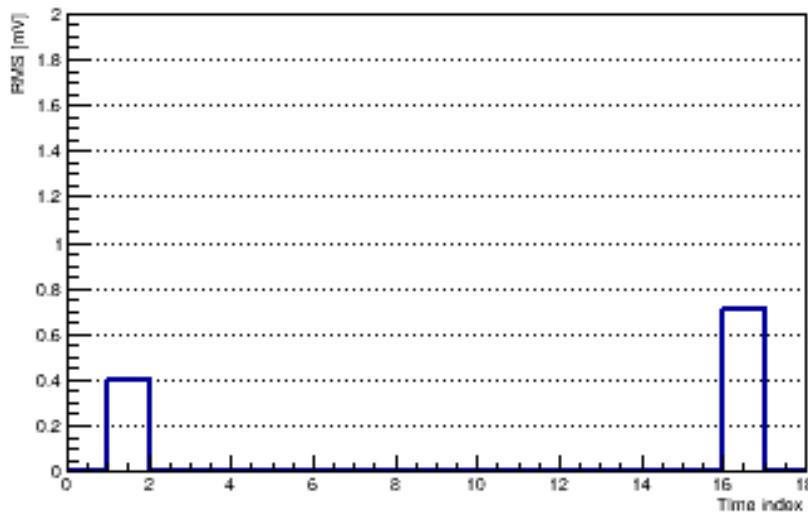


Time varying bins 20

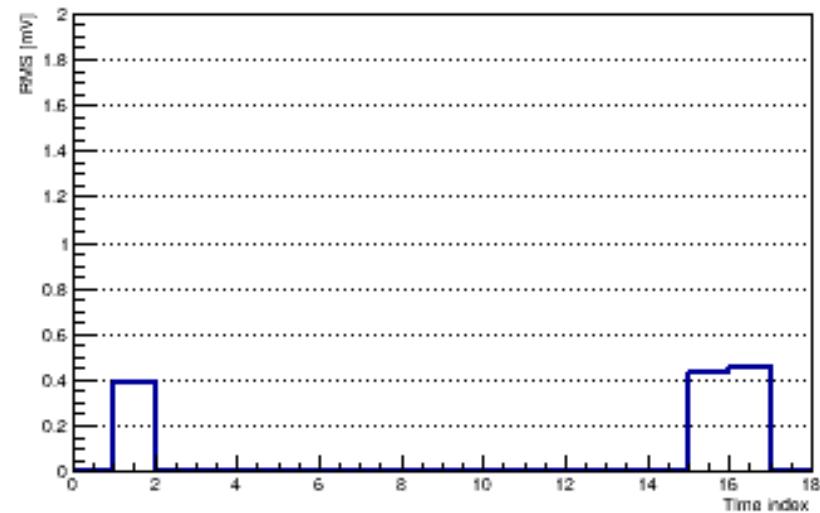


Time varying bins 21

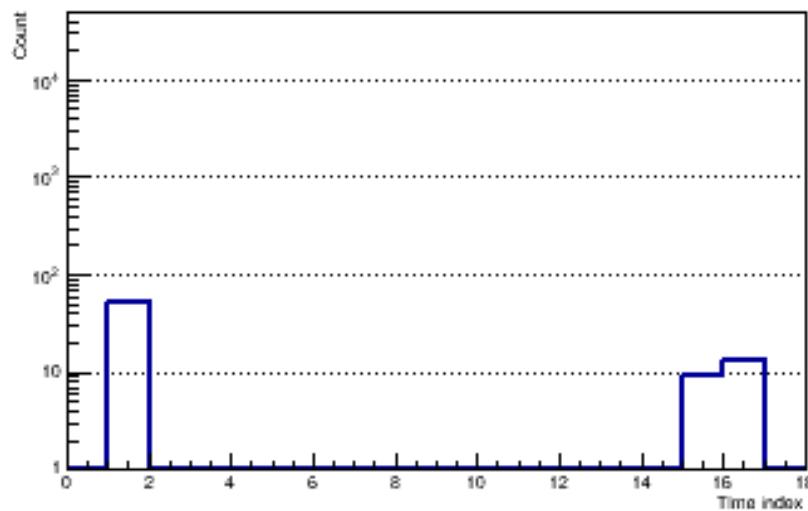
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 71



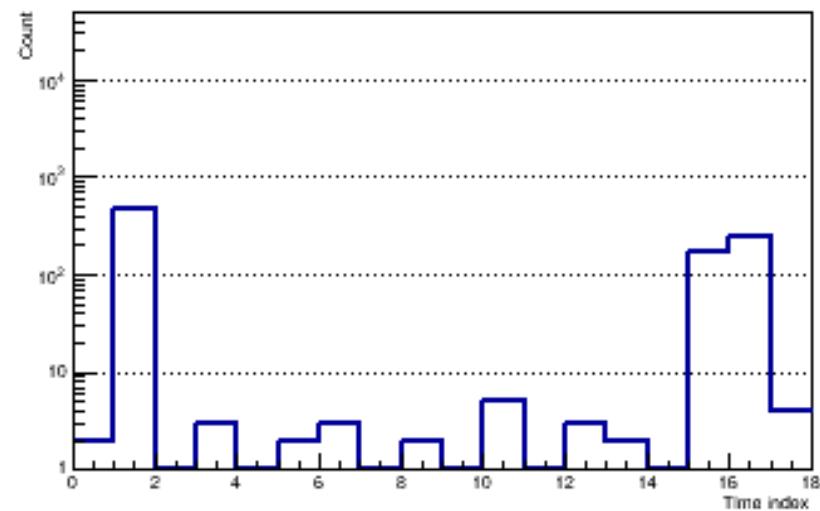
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 72



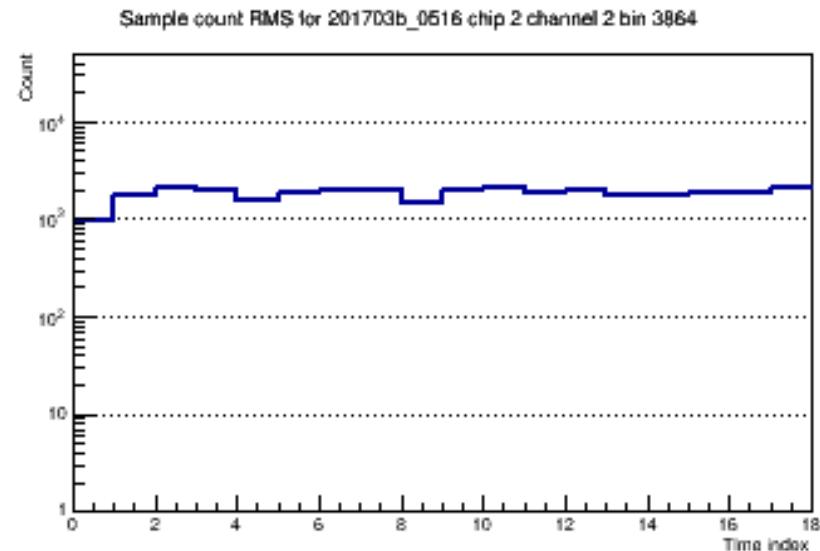
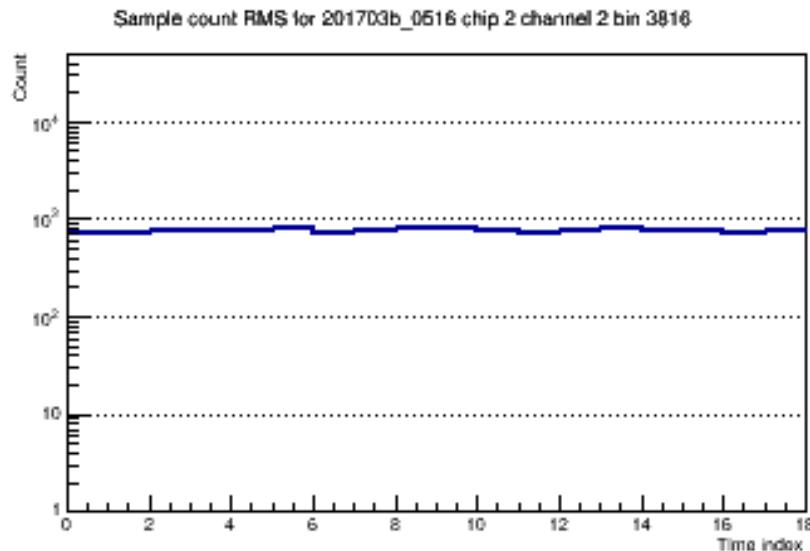
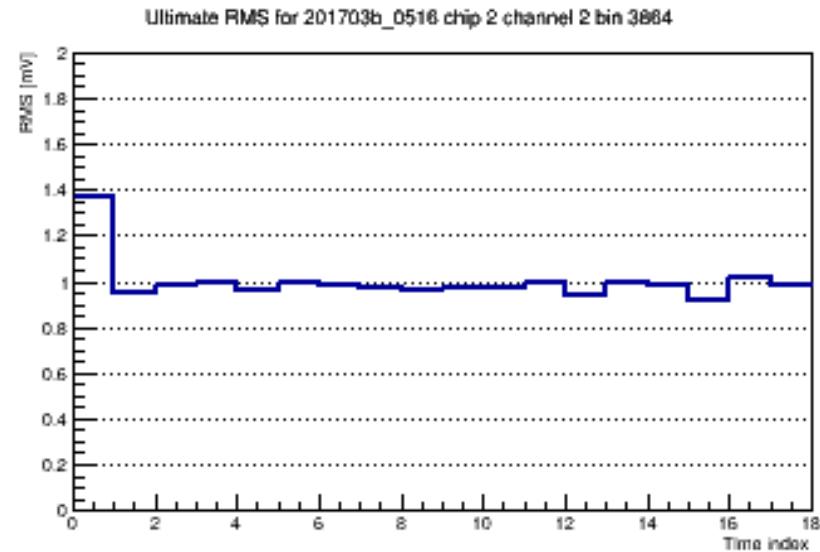
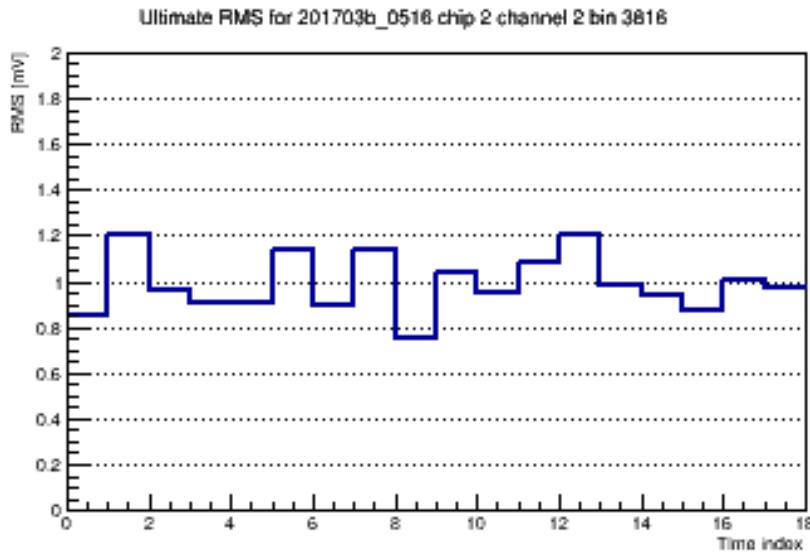
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 71



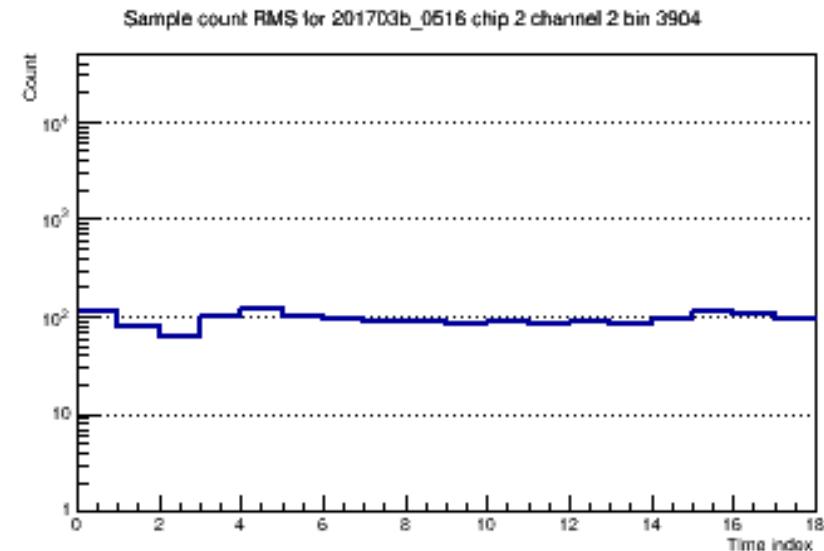
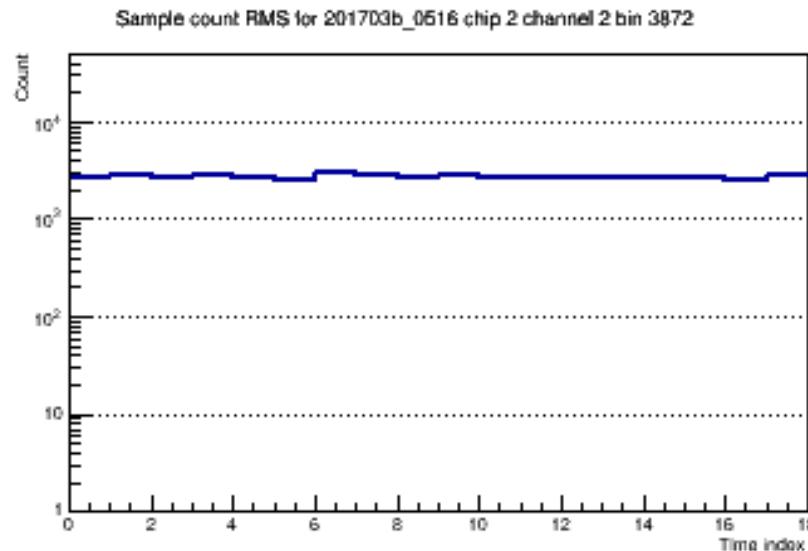
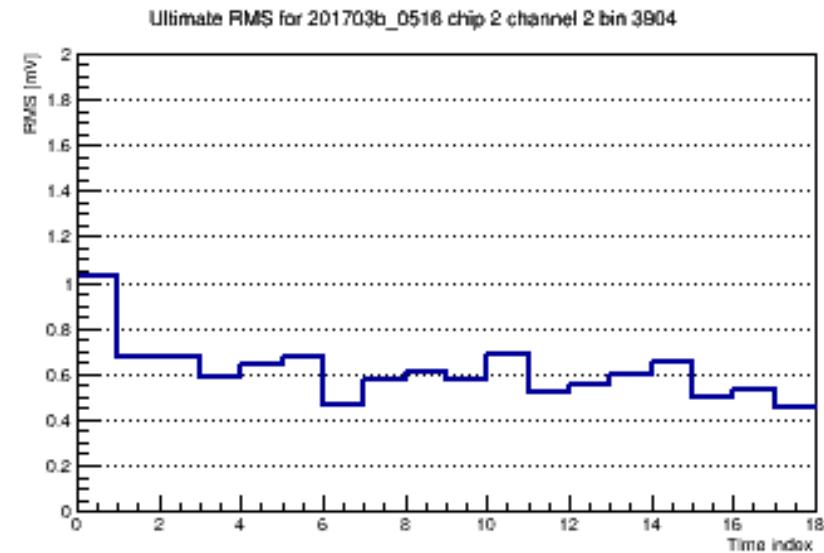
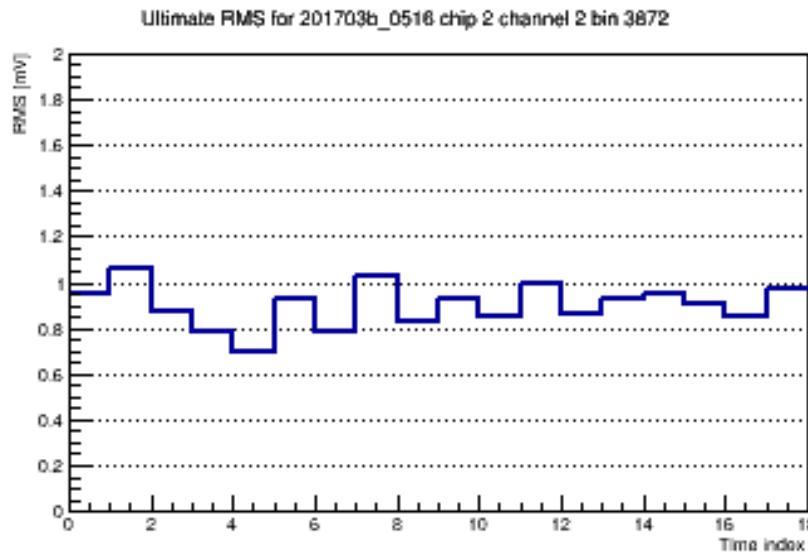
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 72



Time varying bins 22

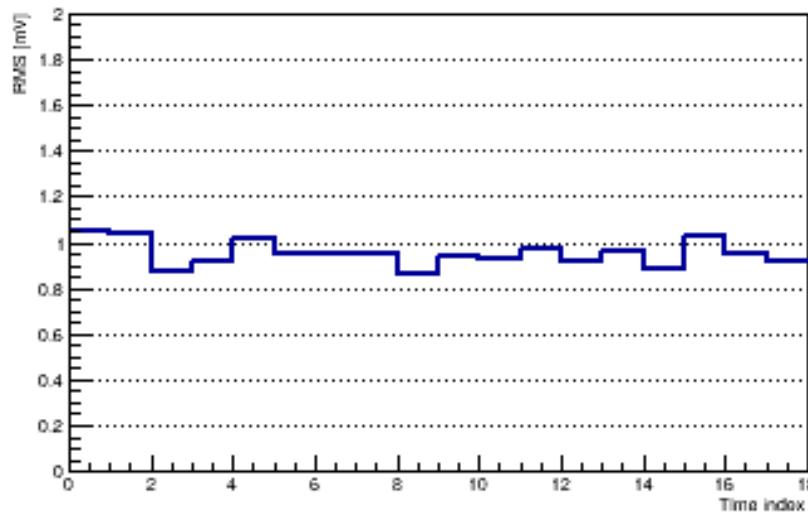


Time varying bins 23

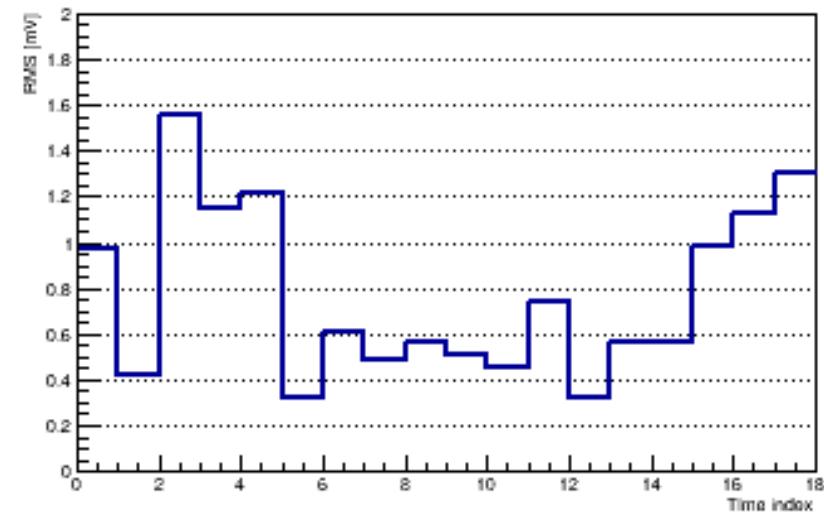


Time varying bins 24

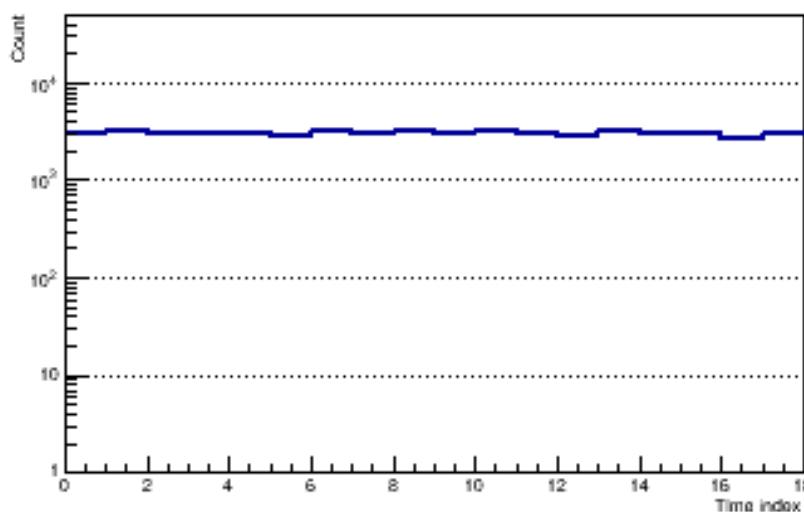
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 3936



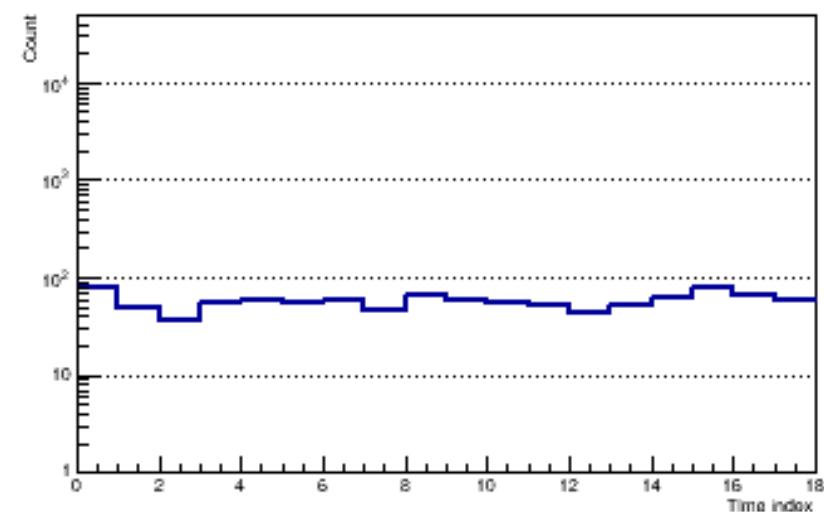
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 4032



Sample count RMS for 201703b_0516 chip 2 channel 2 bin 3936

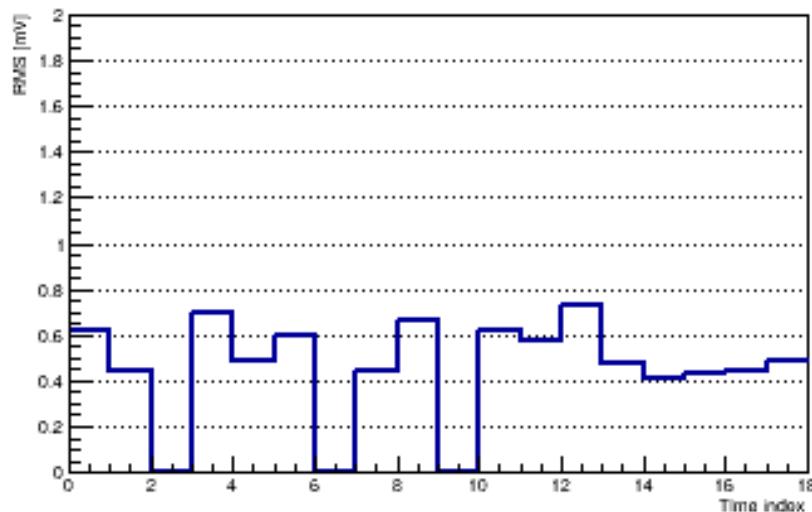


Sample count RMS for 201703b_0516 chip 2 channel 2 bin 4032

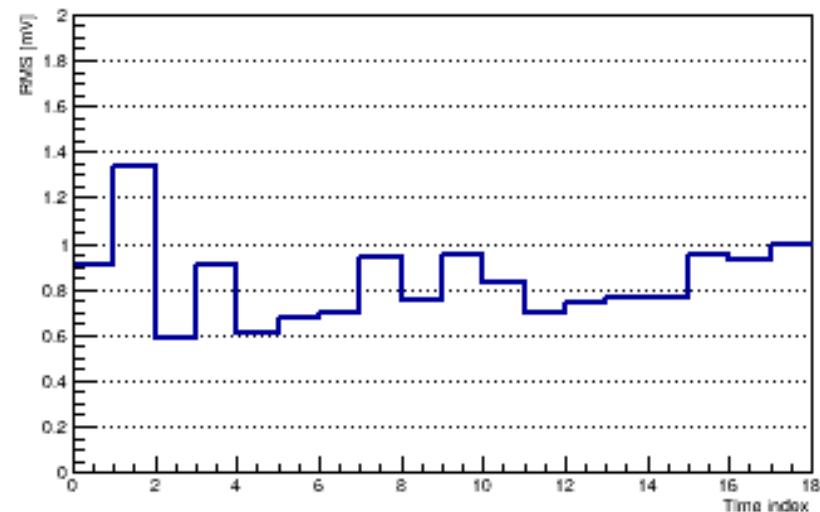


Time varying bins 25

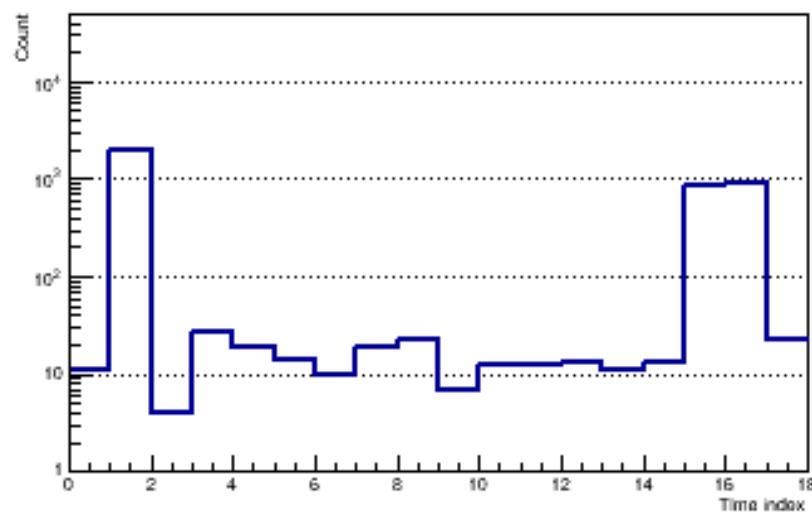
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 73



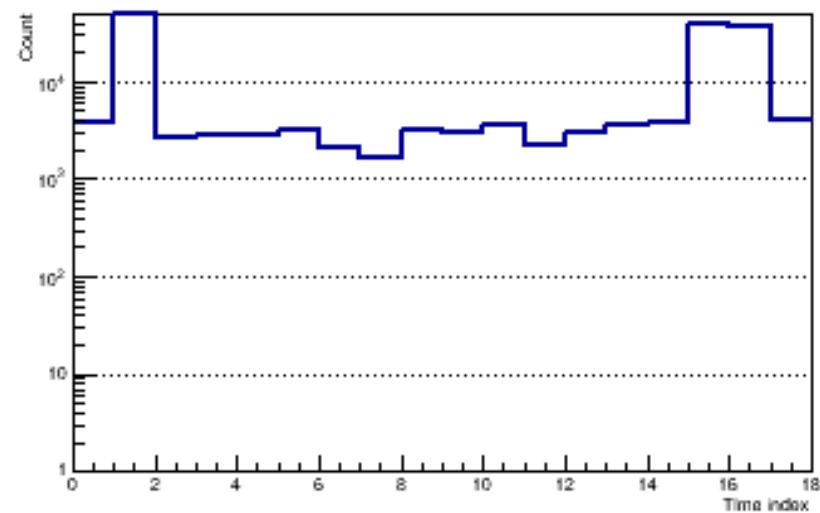
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 128



Sample count RMS for 201703b_0516 chip 2 channel 2 bin 73

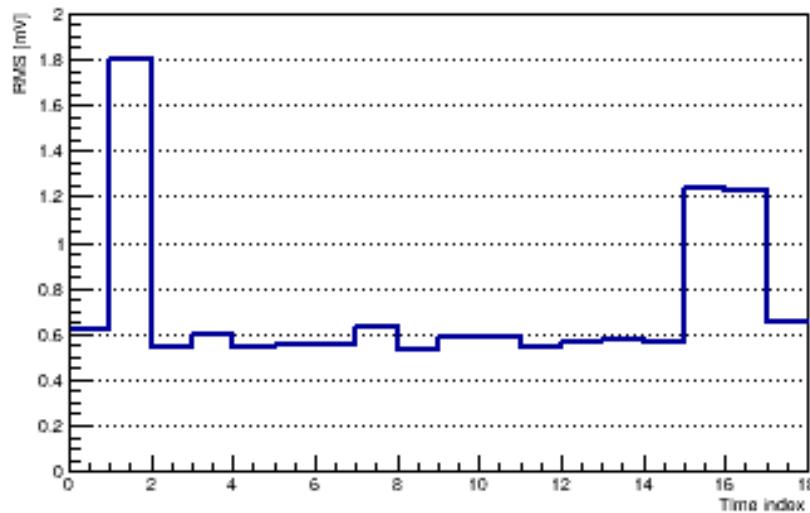


Sample count RMS for 201703b_0516 chip 2 channel 2 bin 128

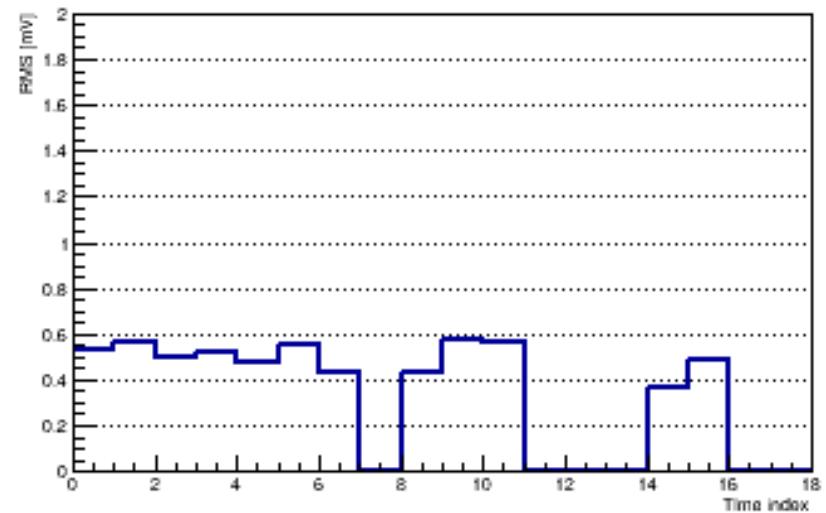


Time varying bins 26

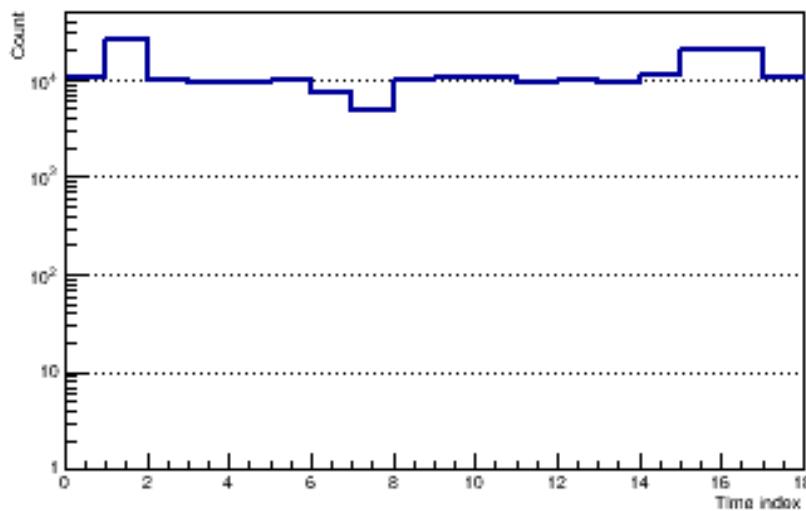
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 129



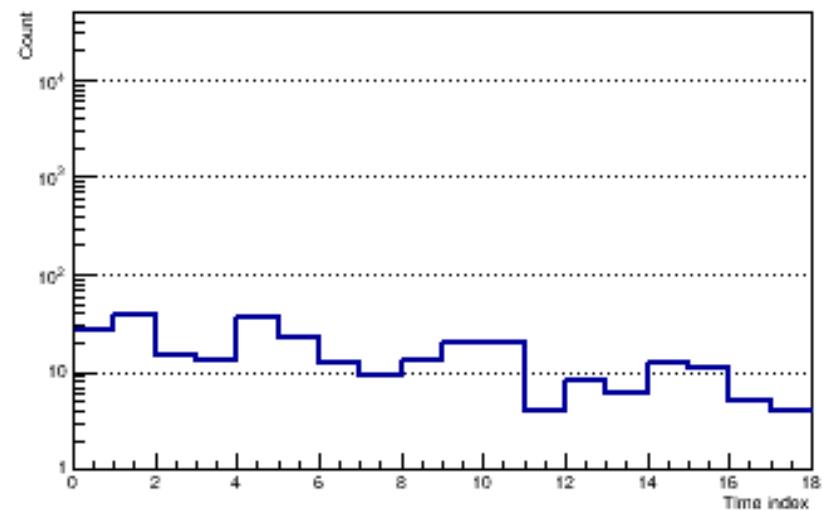
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 191



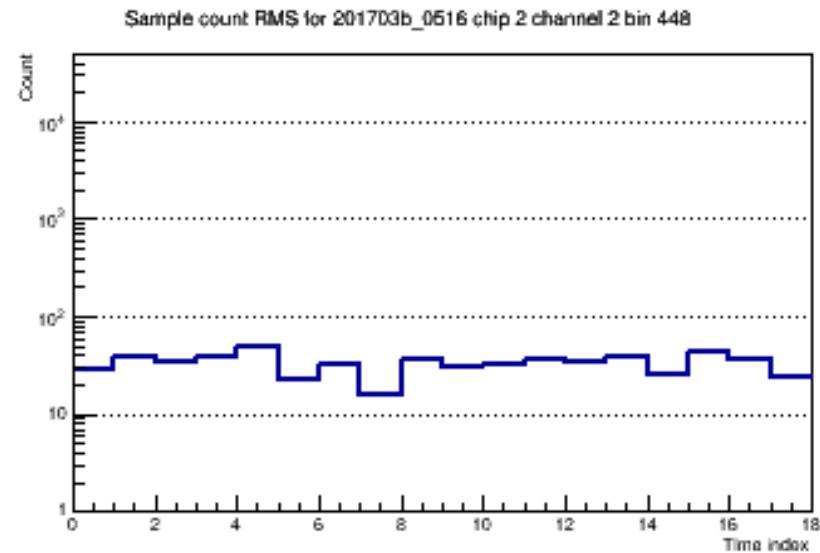
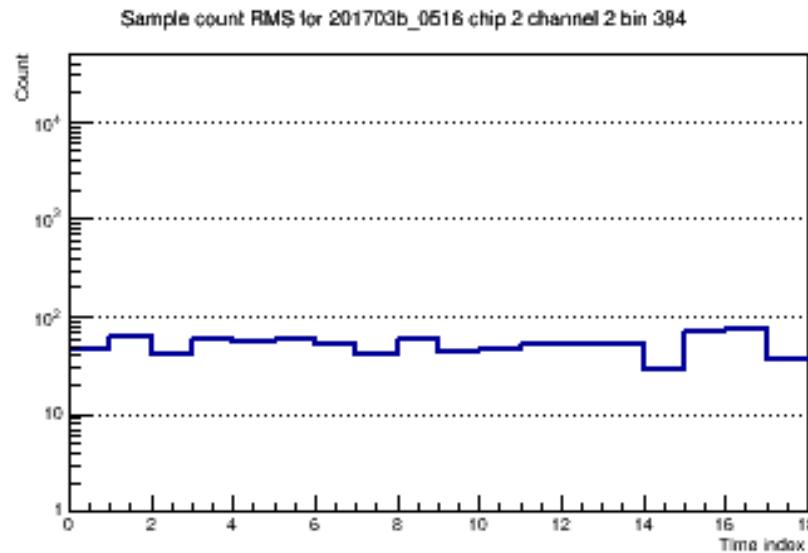
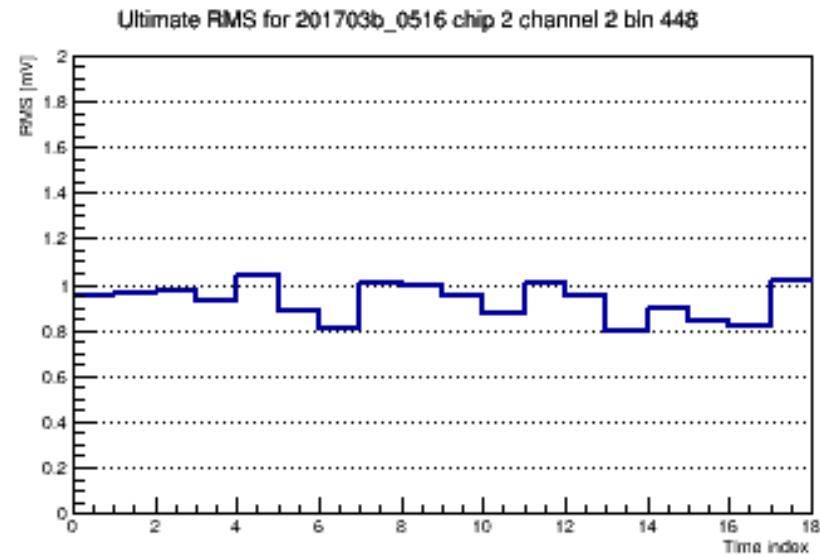
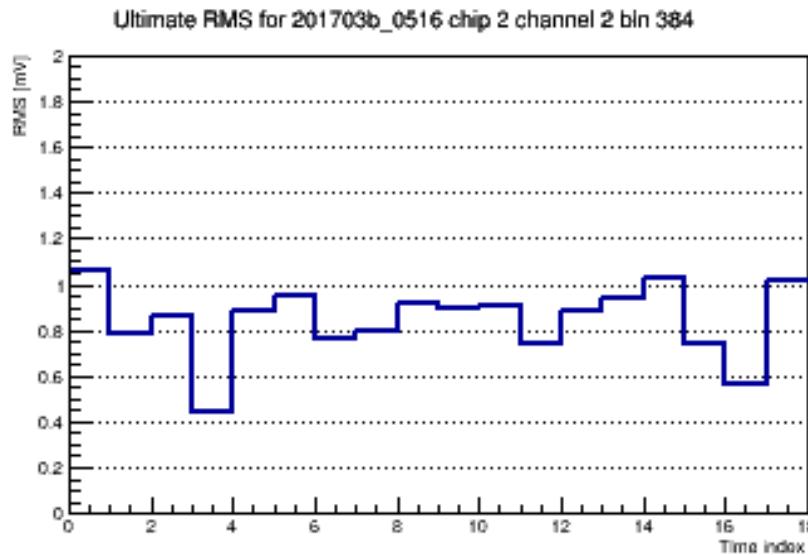
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 129



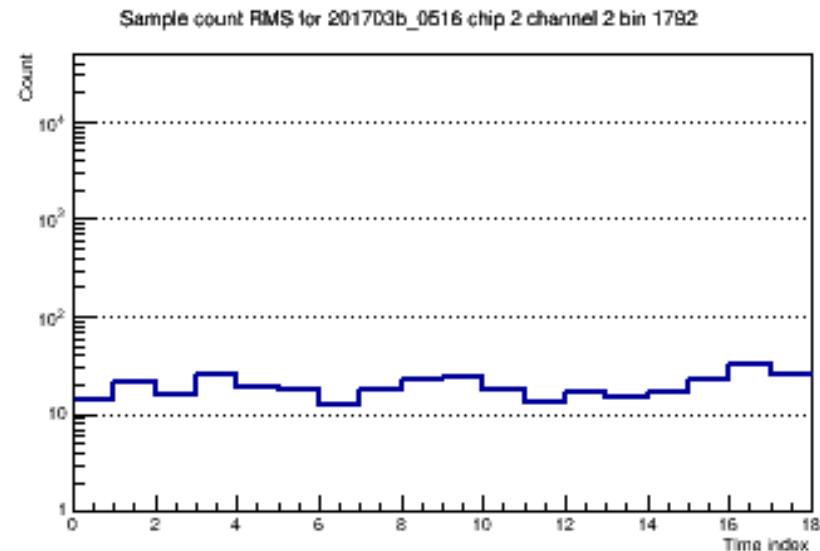
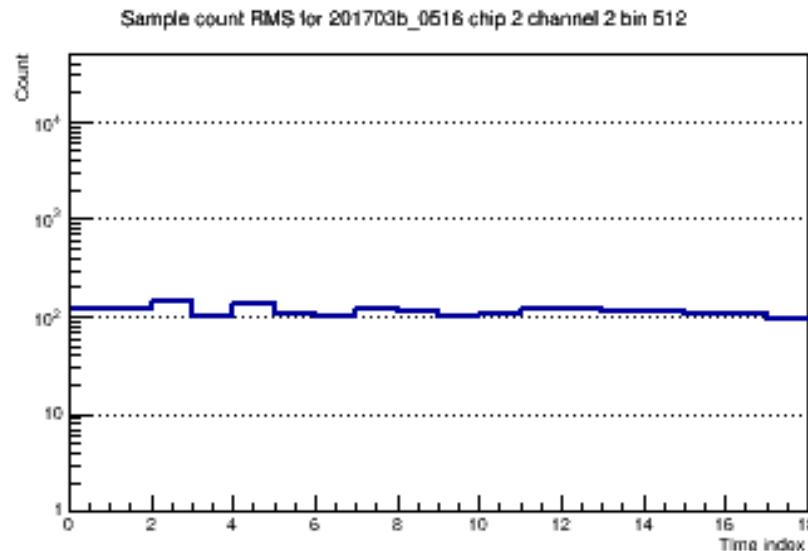
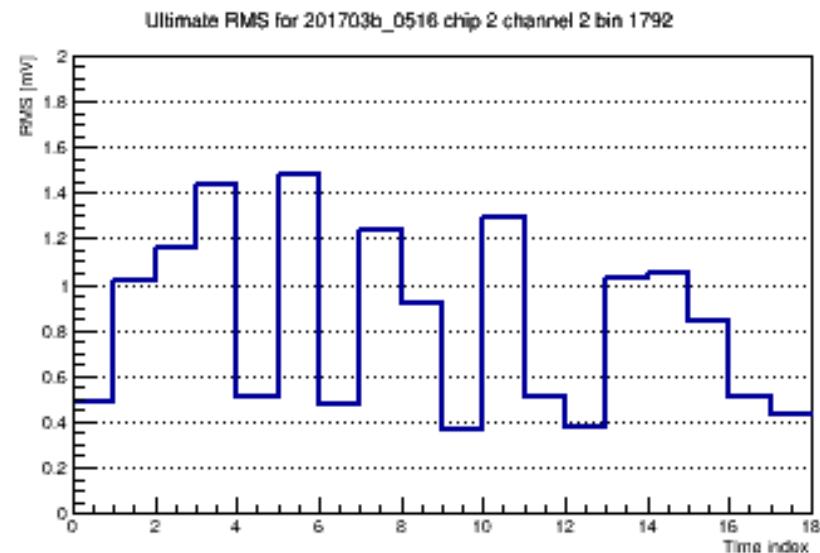
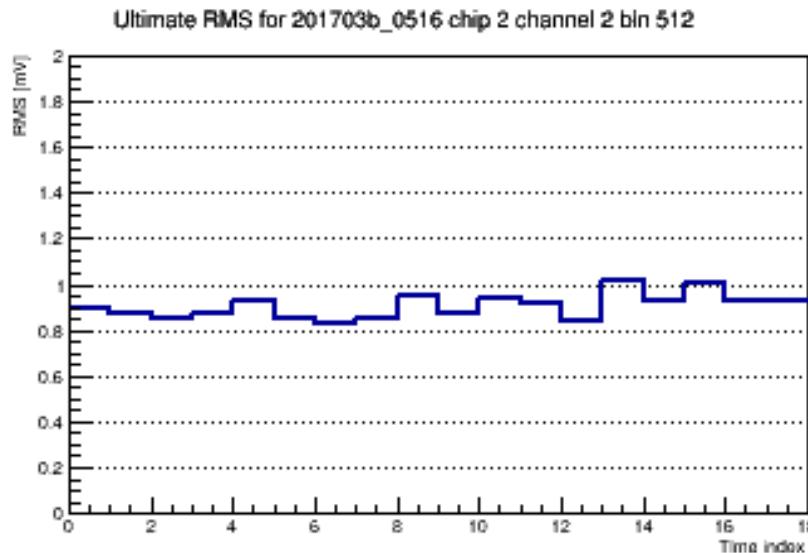
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 191



Time varying bins 27

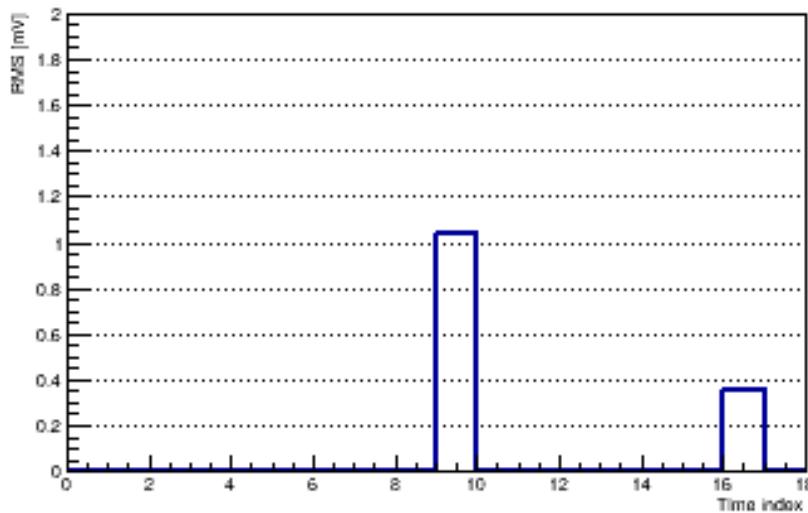


Time varying bins 28

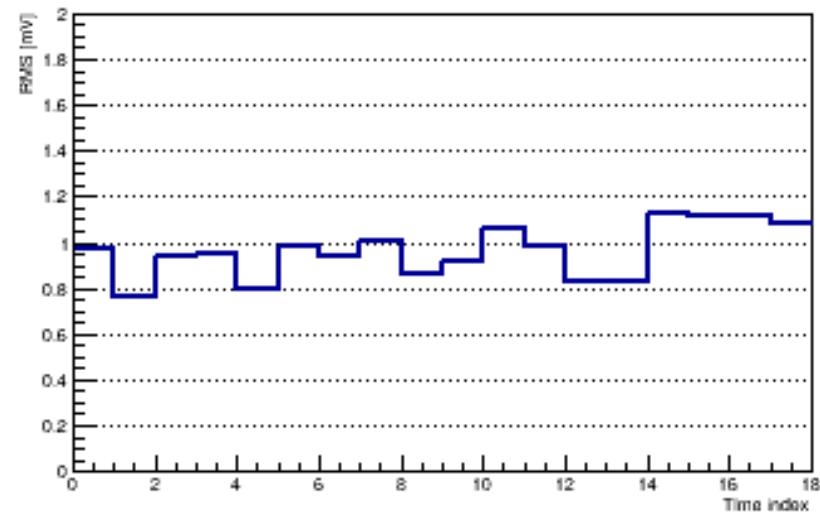


Time varying bins 29

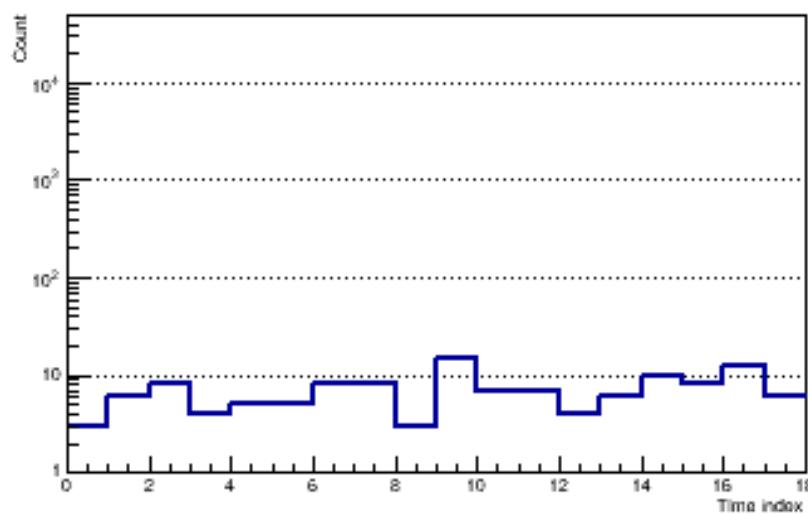
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 1984



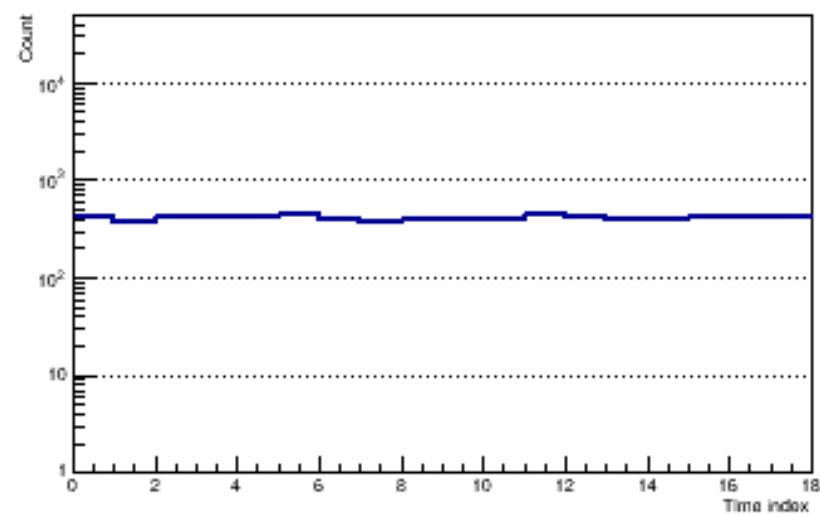
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2008



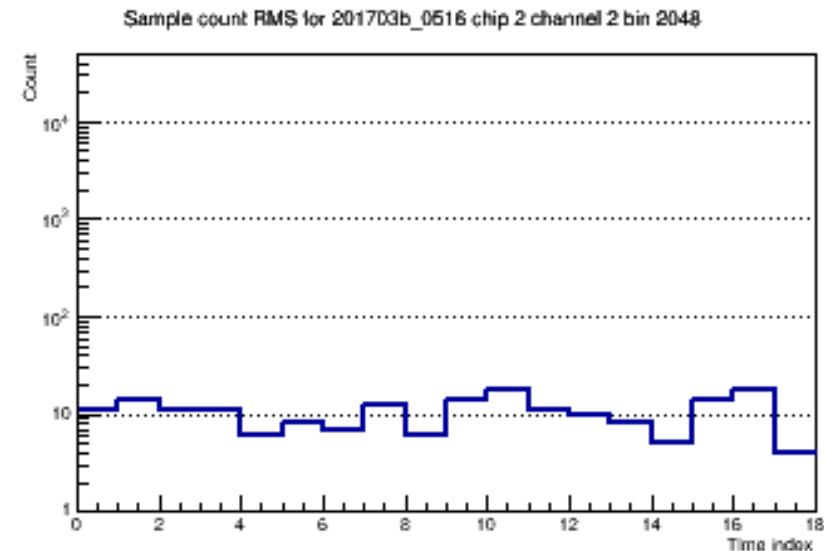
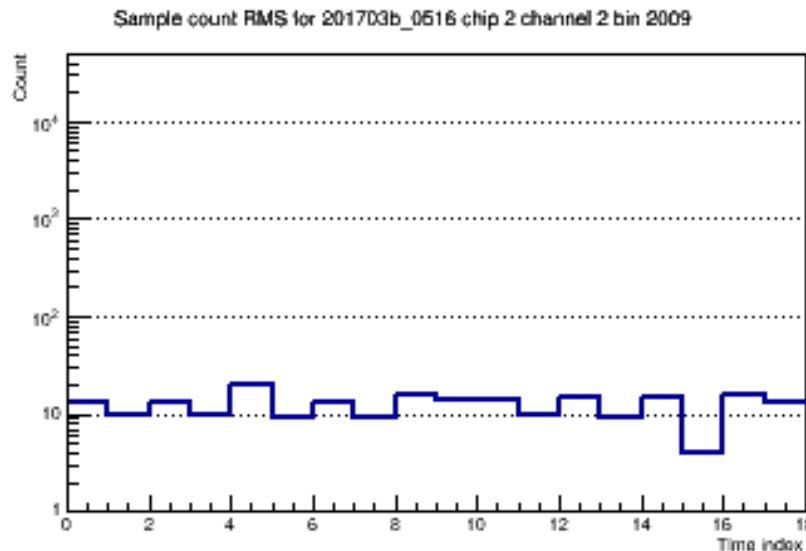
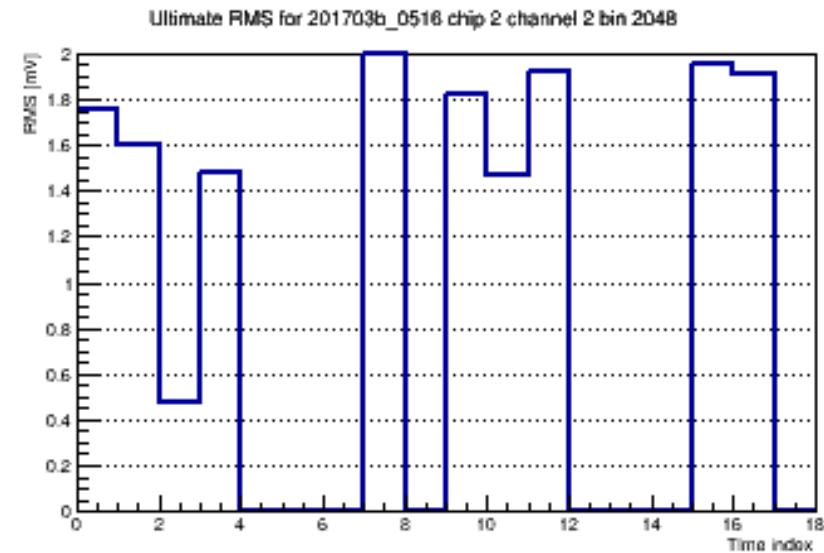
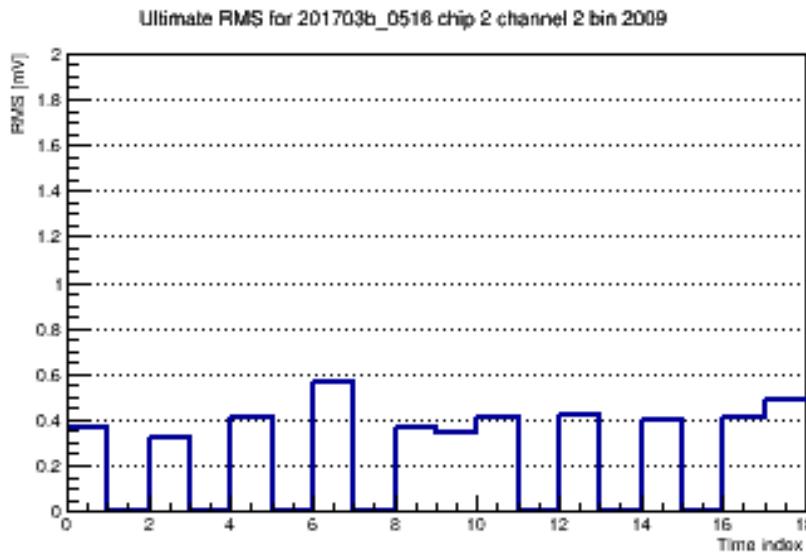
Sample count RMS for 201703b_0516 chip 2 channel 2 bin 1984



Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2008

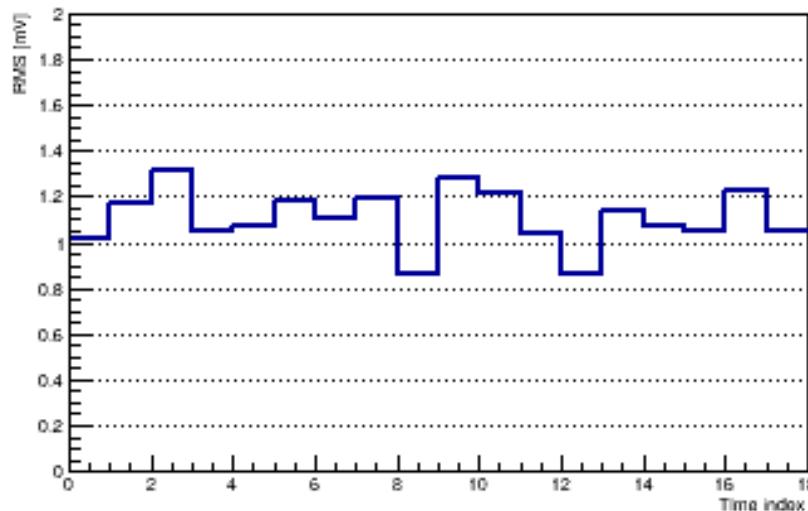


Time varying bins 30

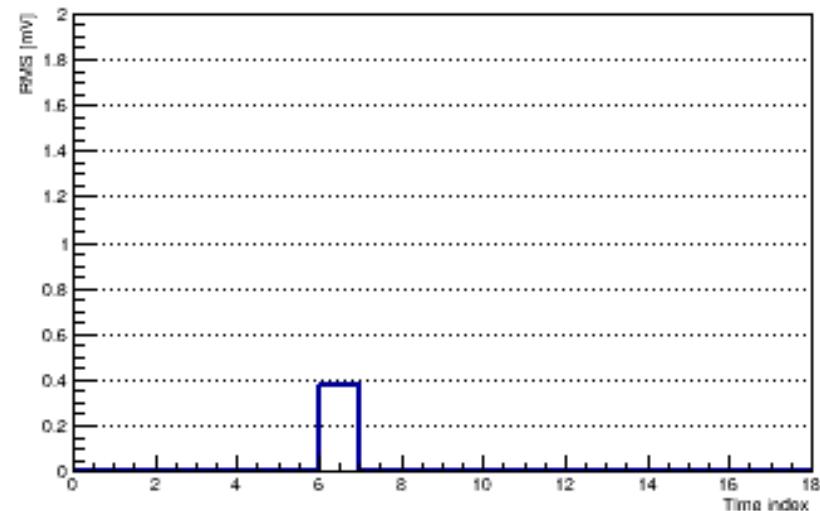


Time varying bins 31

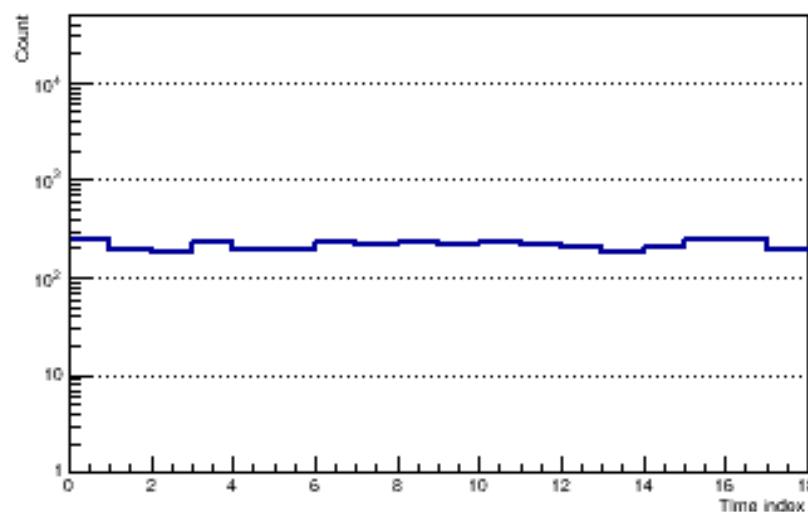
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2072



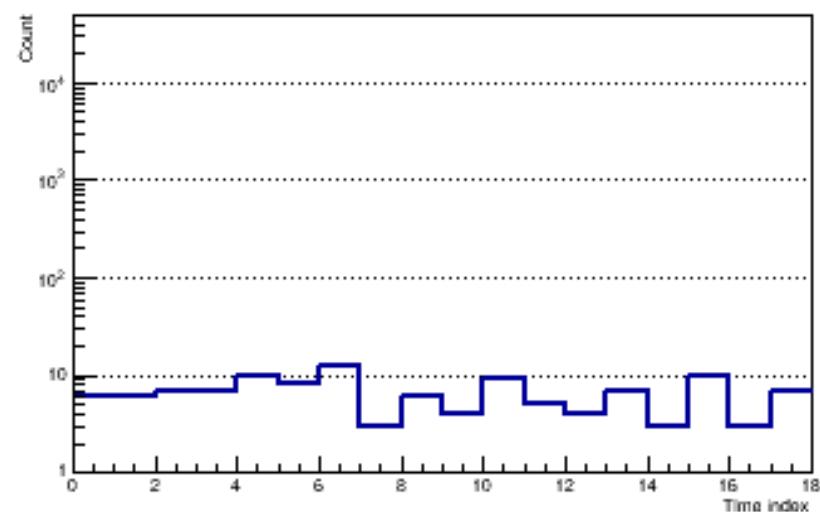
Ultimate RMS for 201703b_0516 chip 2 channel 2 bin 2073



Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2072

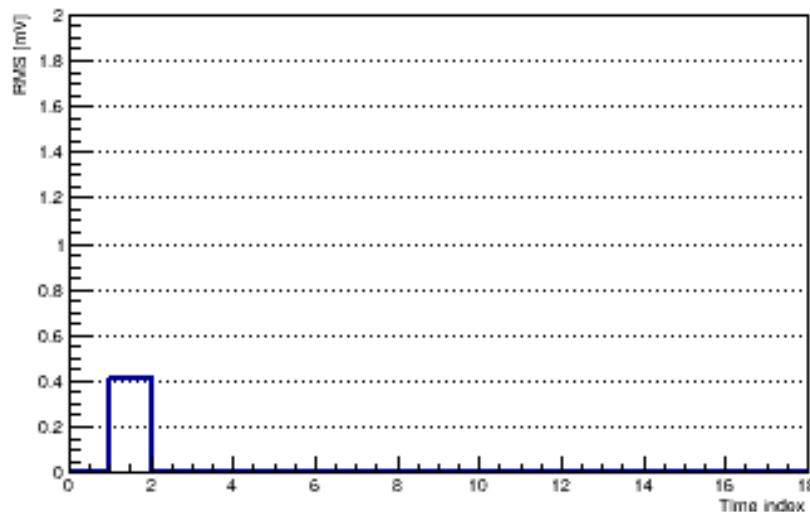


Sample count RMS for 201703b_0516 chip 2 channel 2 bin 2073

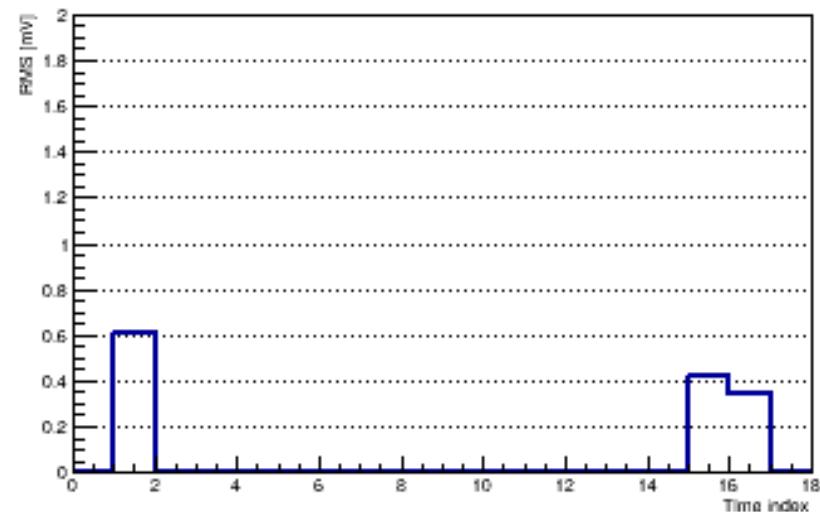


Time varying bins 32

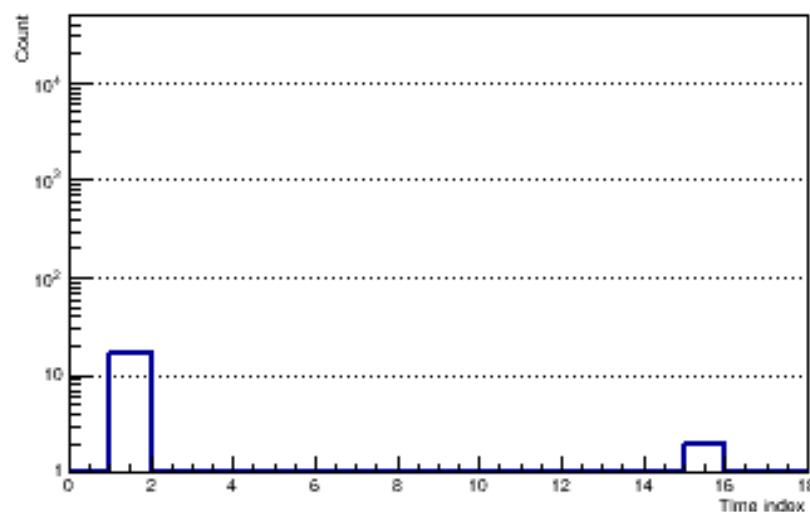
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 69



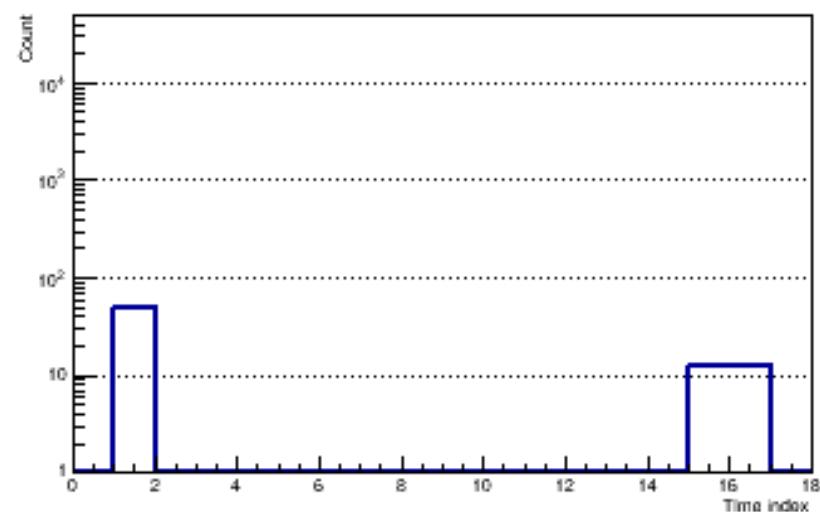
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 70



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 69

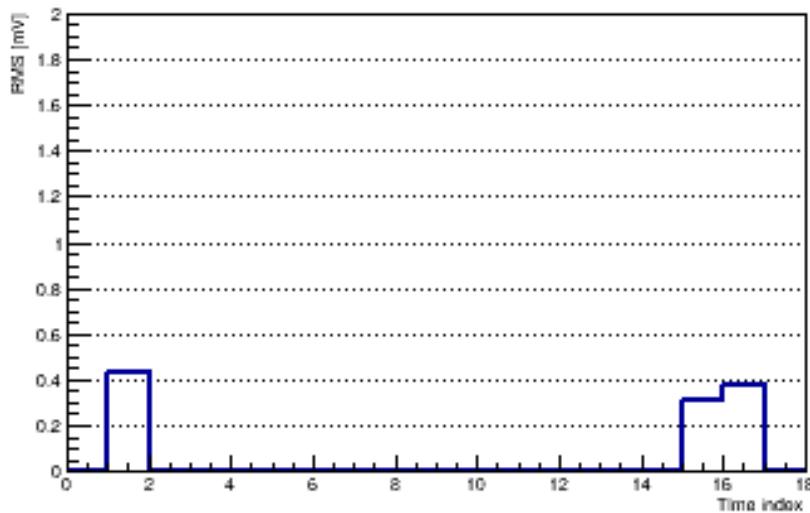


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 70

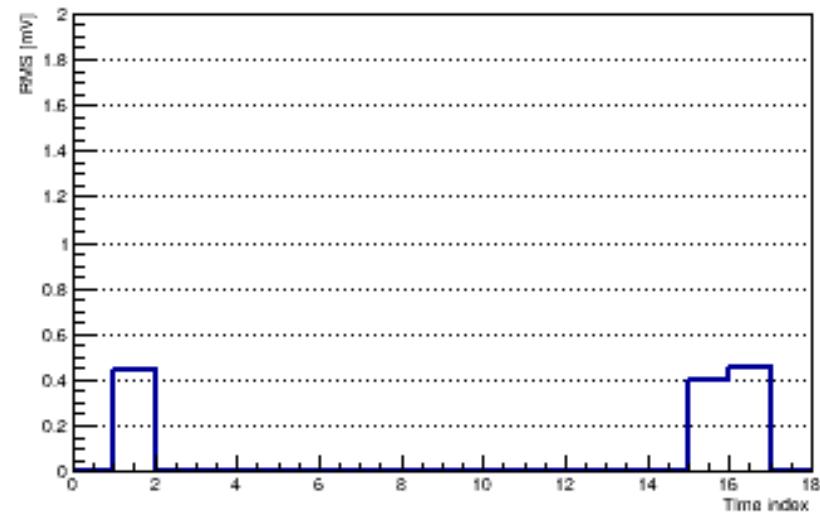


Time varying bins 33

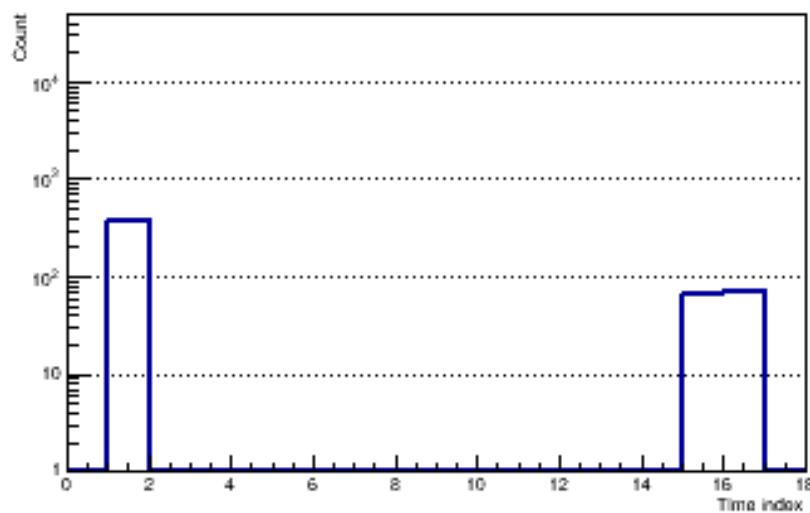
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 71



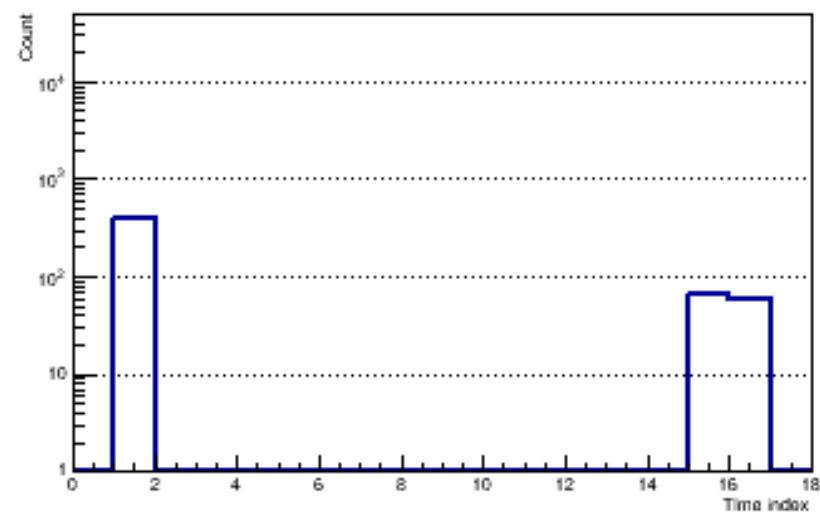
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 72



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 71

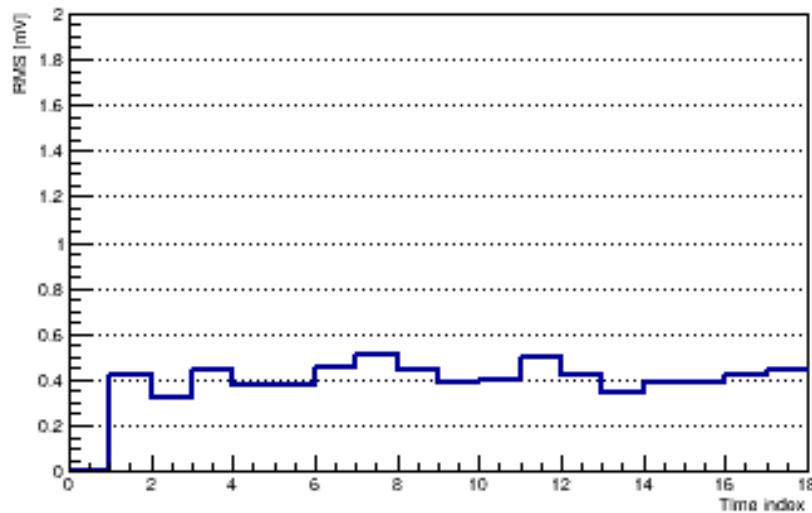


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 72

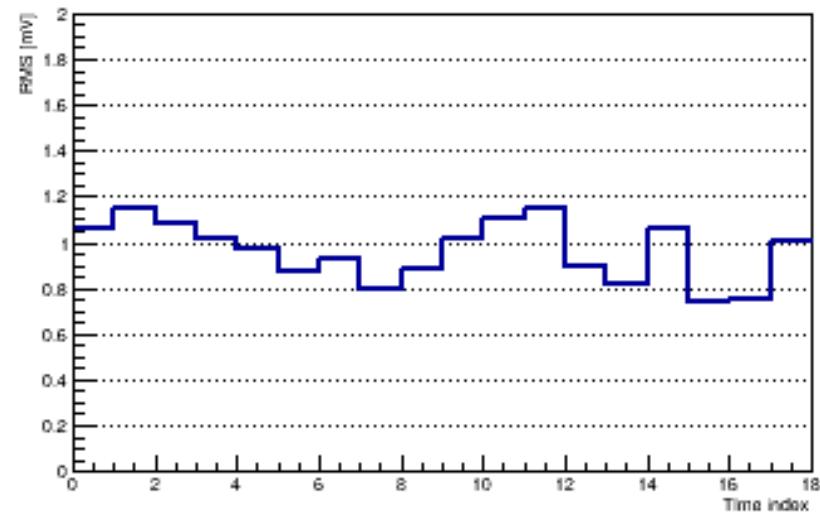


Time varying bins 34

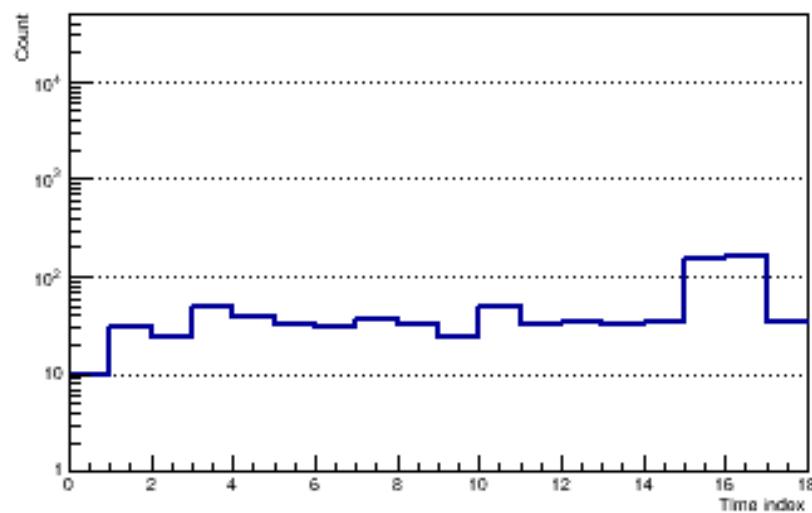
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 321



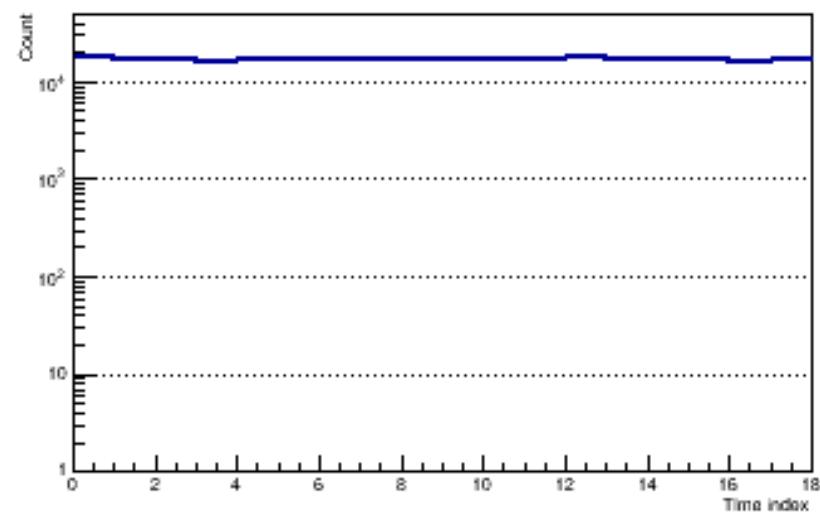
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 1855



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 321

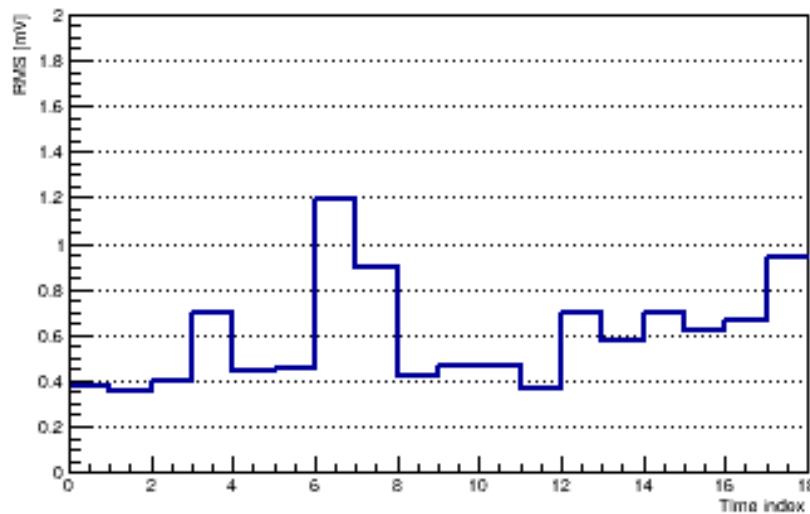


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 1855

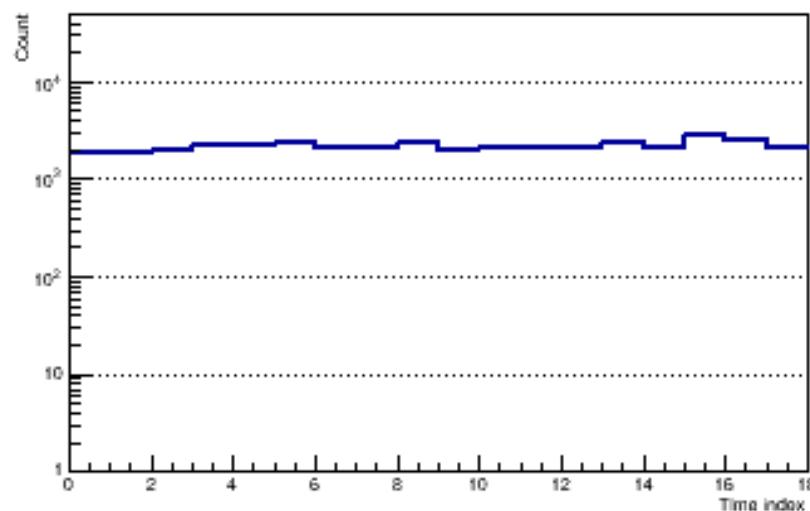


Time varying bins 35

Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 3456

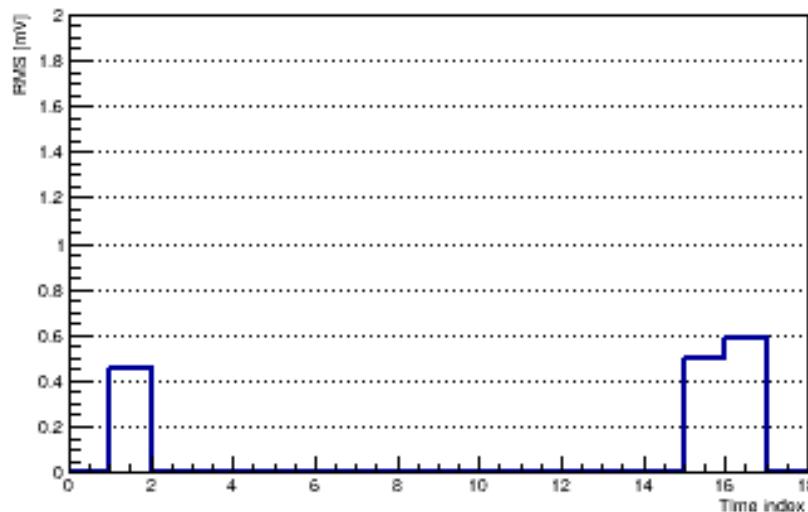


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 3456

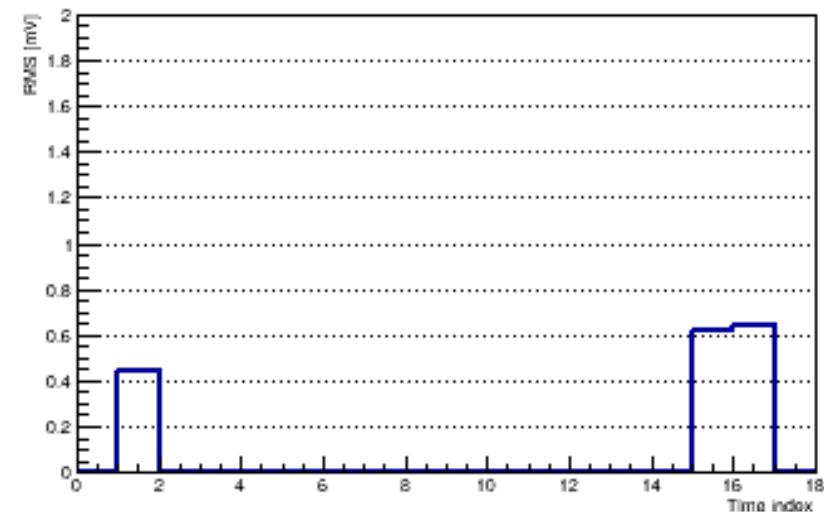


Time varying bins 36

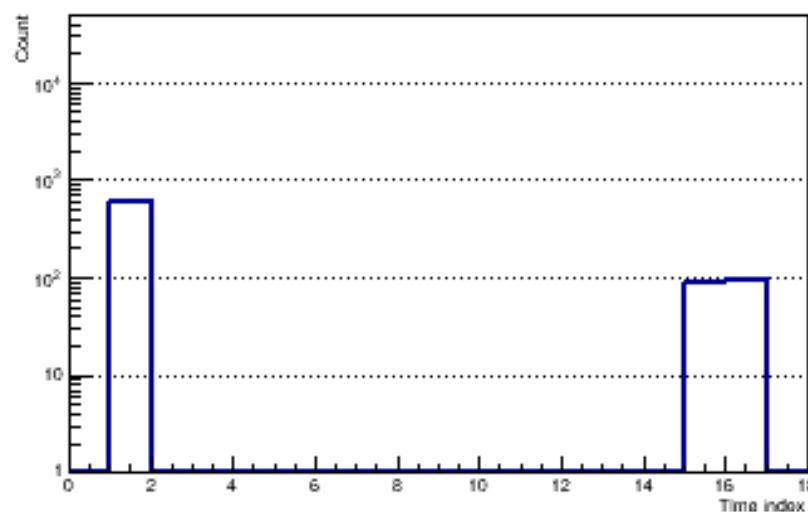
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 73



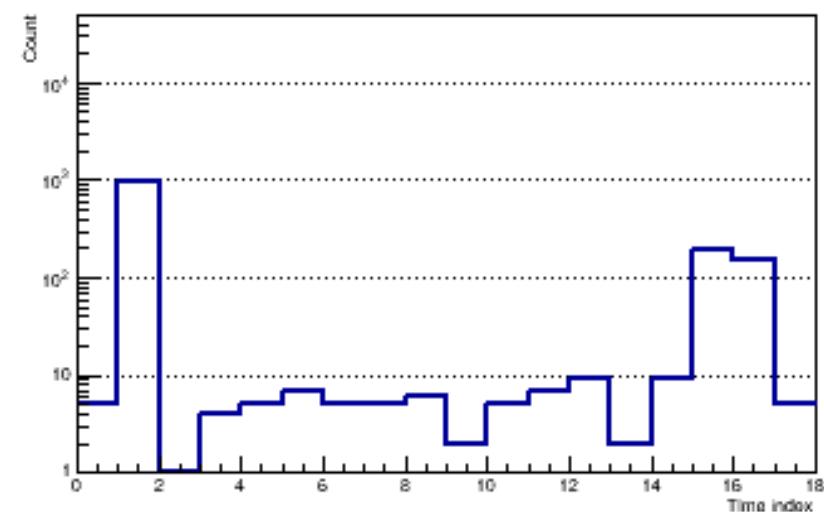
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 74



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 73

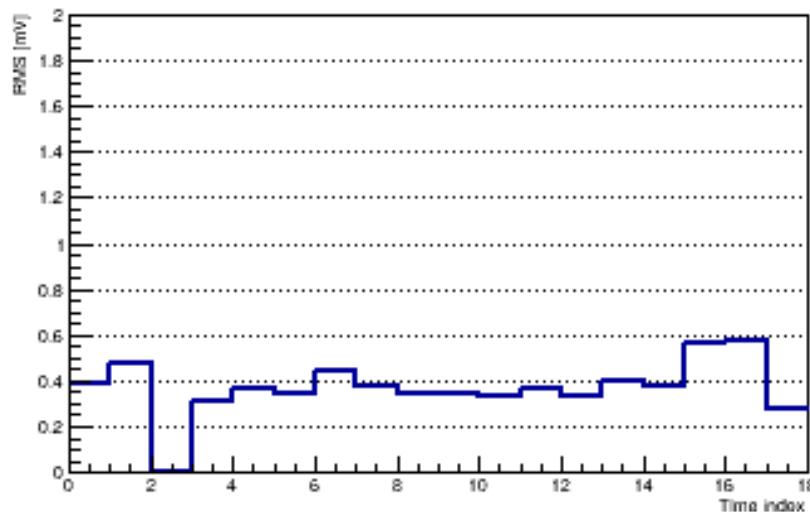


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 74

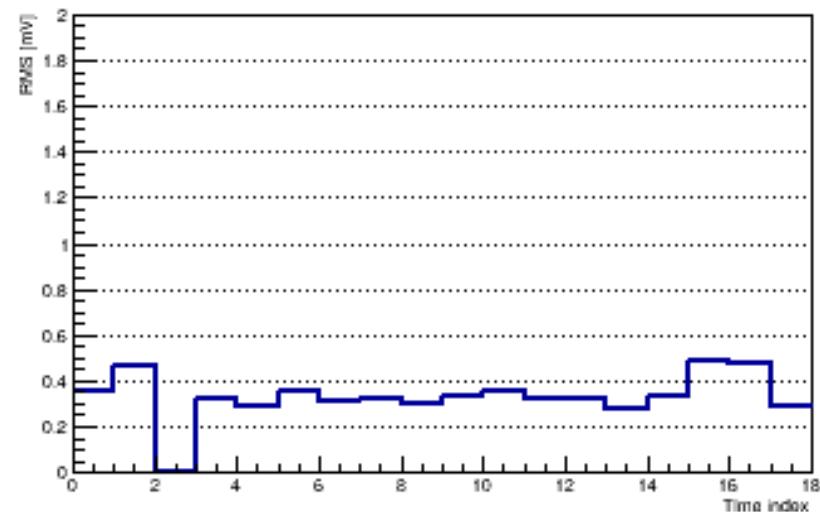


Time varying bins 37

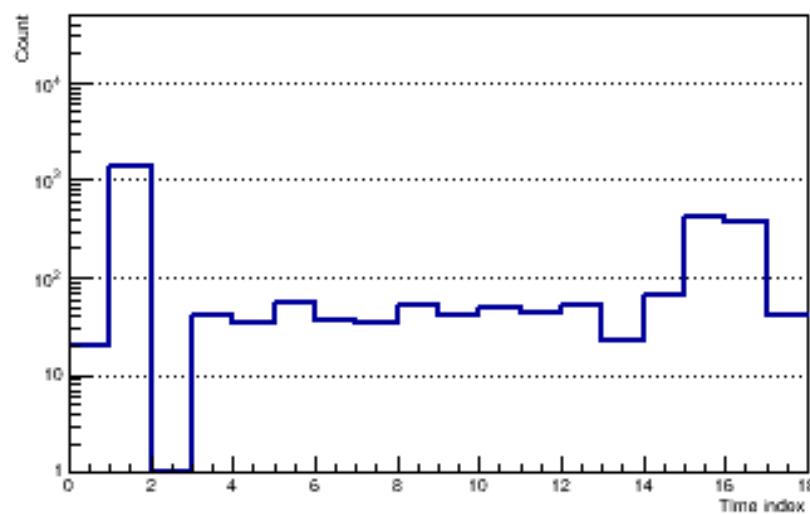
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 75



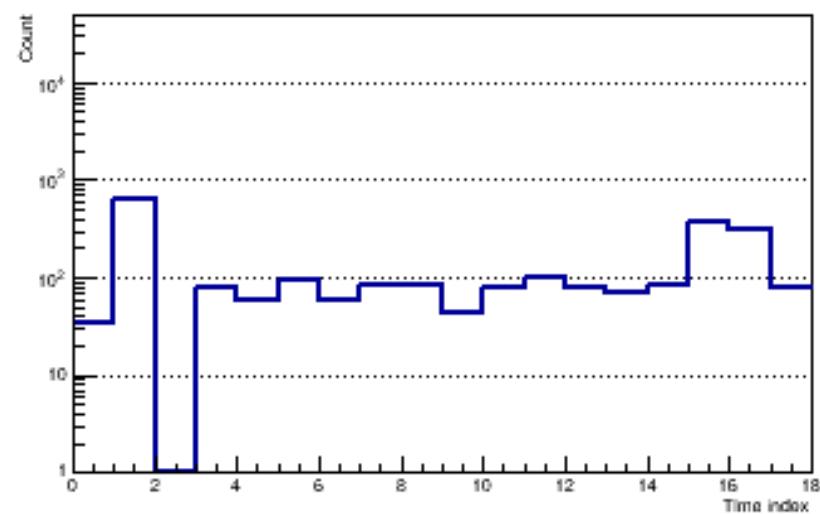
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 76



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 75

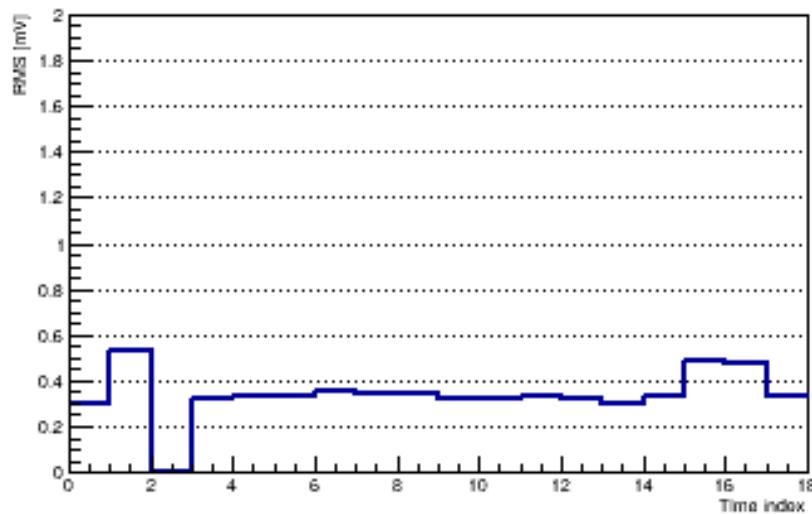


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 76

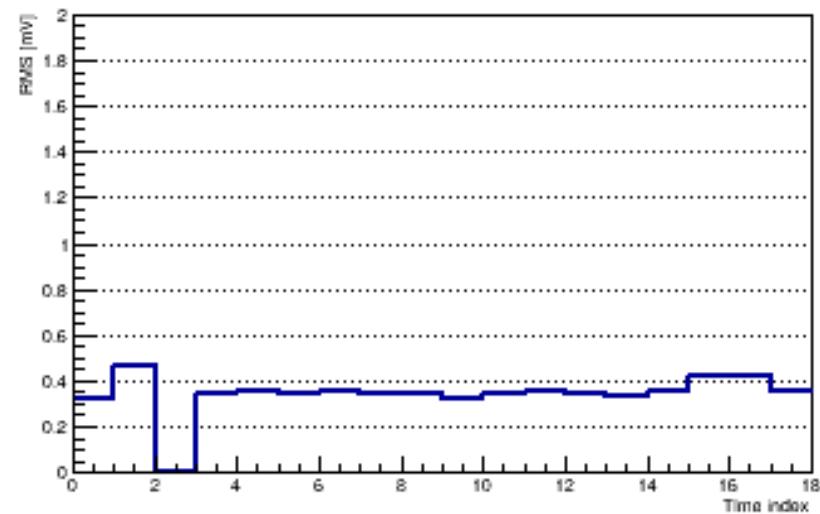


Time varying bins 38

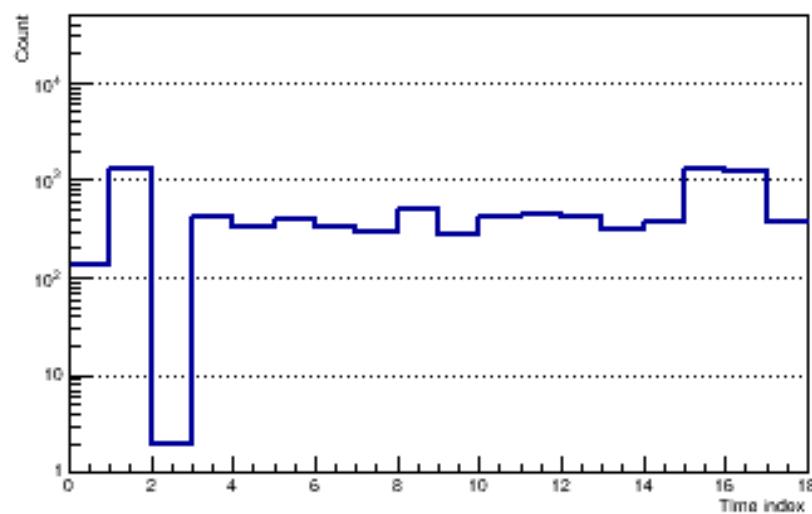
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 77



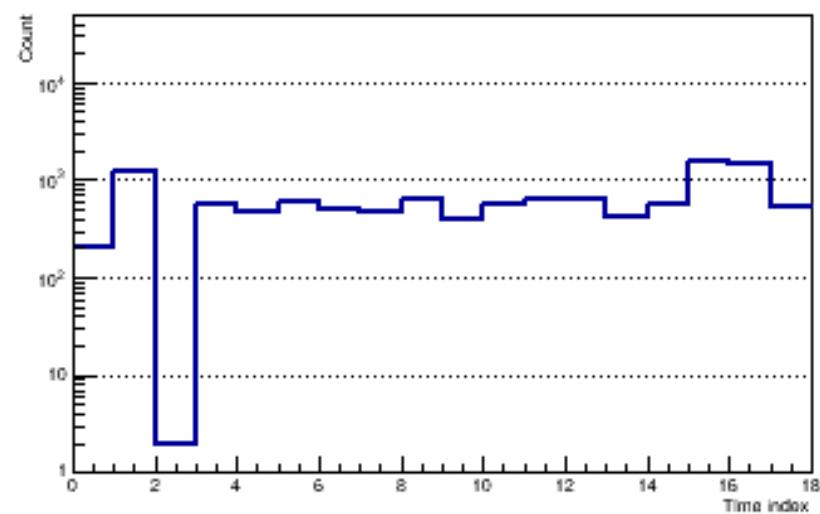
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 78



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 77

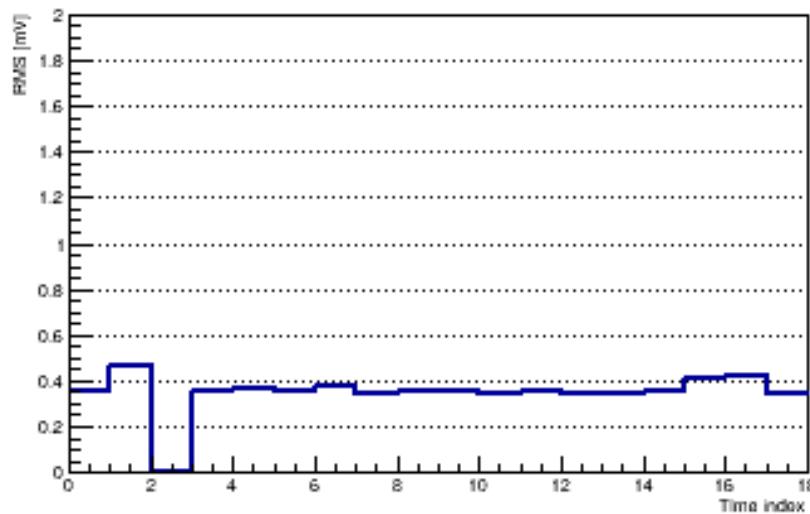


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 78

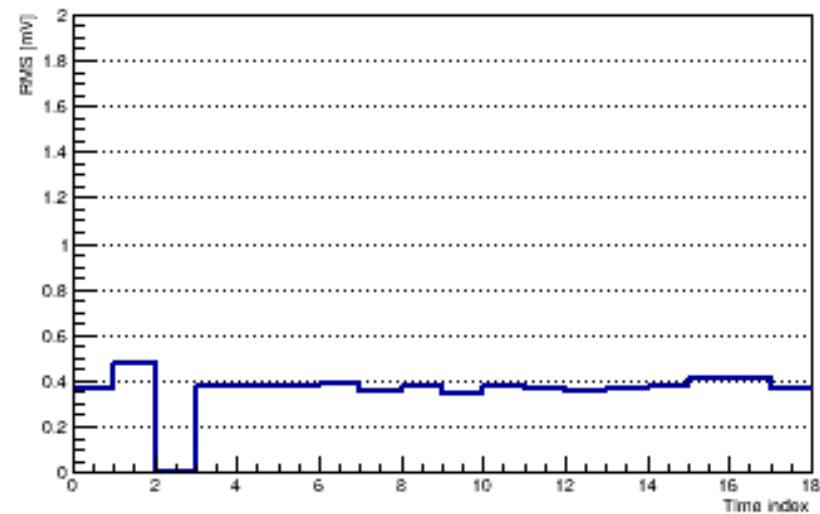


Time varying bins 39

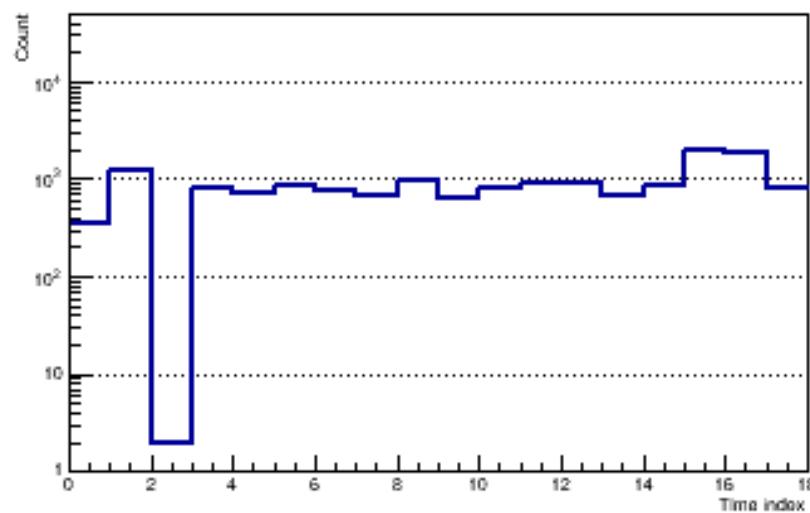
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 79



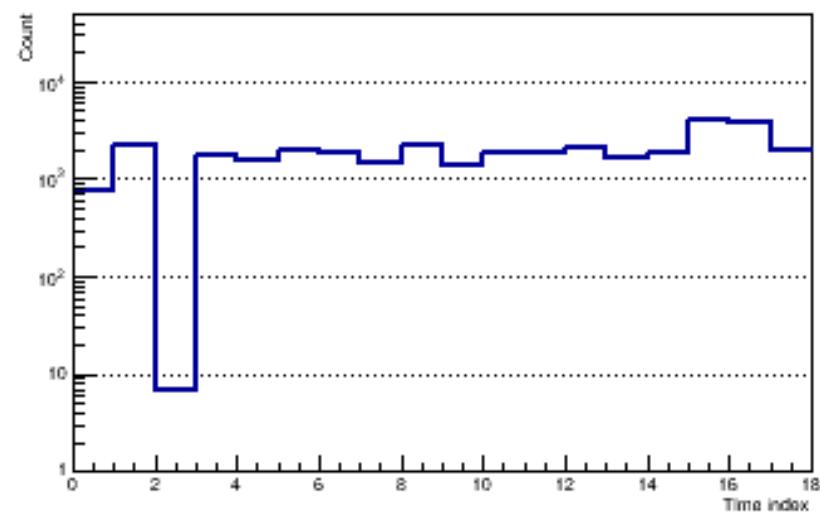
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 80



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 79

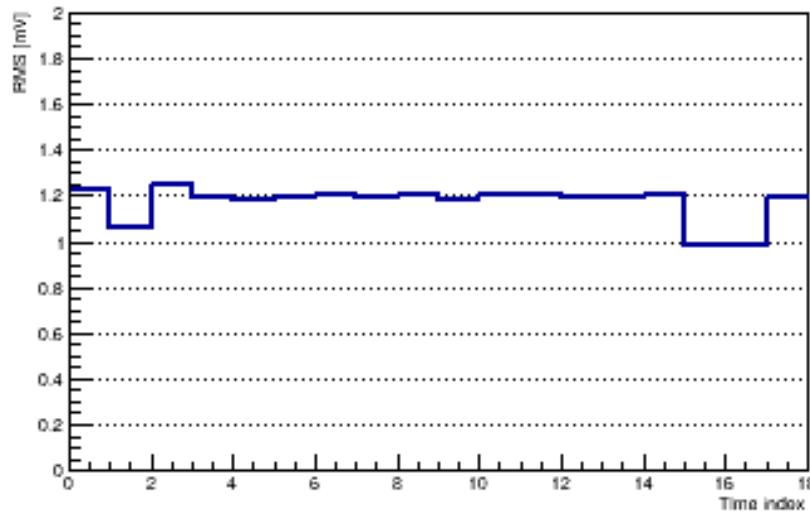


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 80

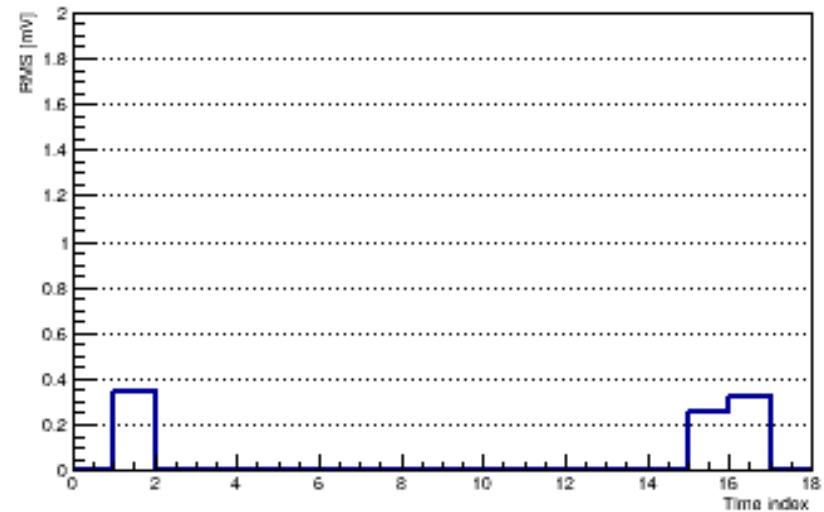


Time varying bins 40

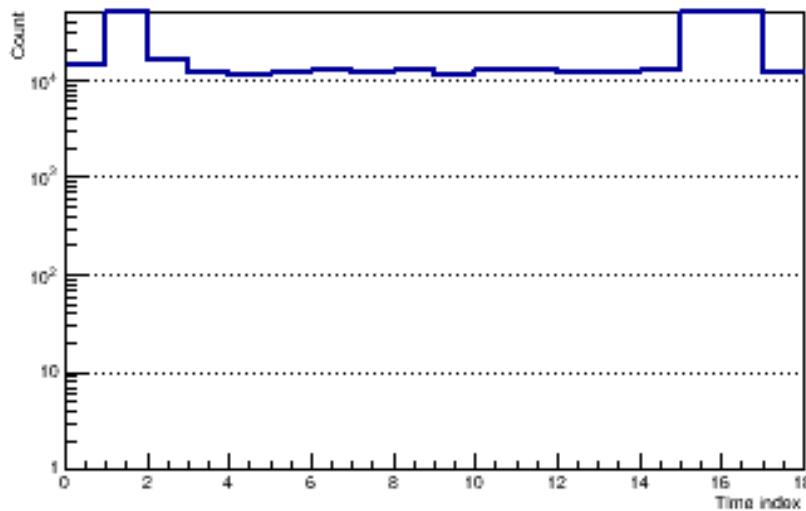
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 127



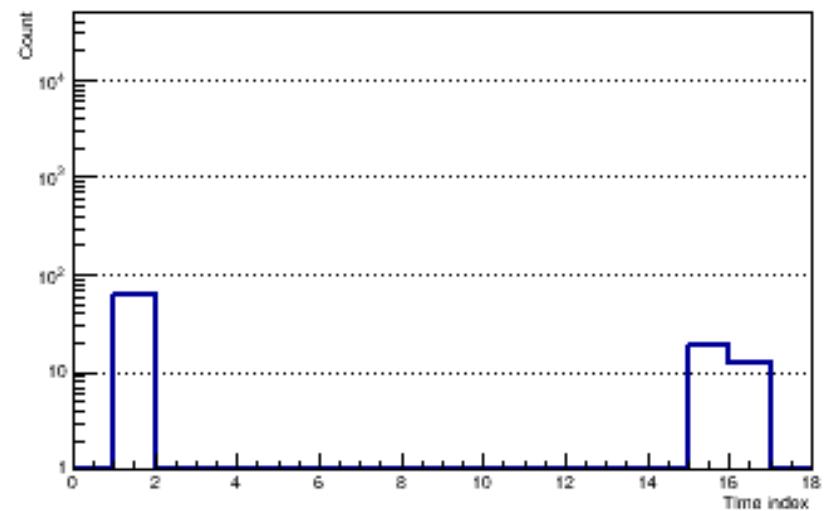
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 130



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 127

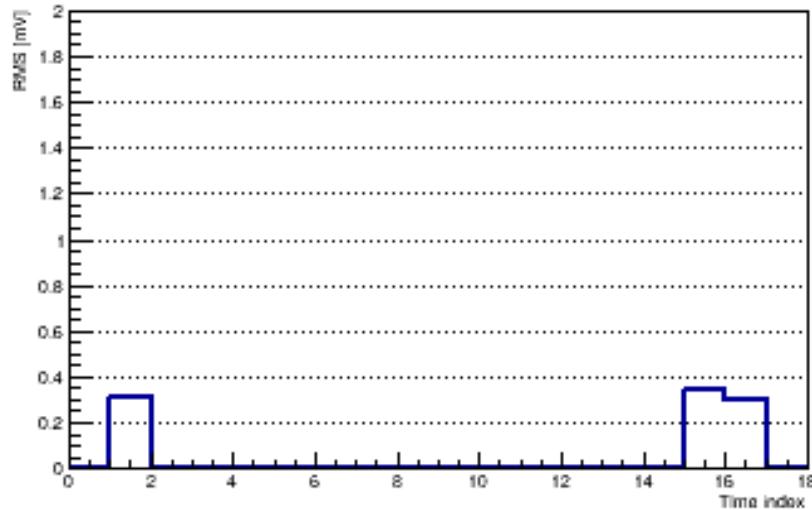


Sample count RMS for 201703b_0516 chip 2 channel 3 bin 130

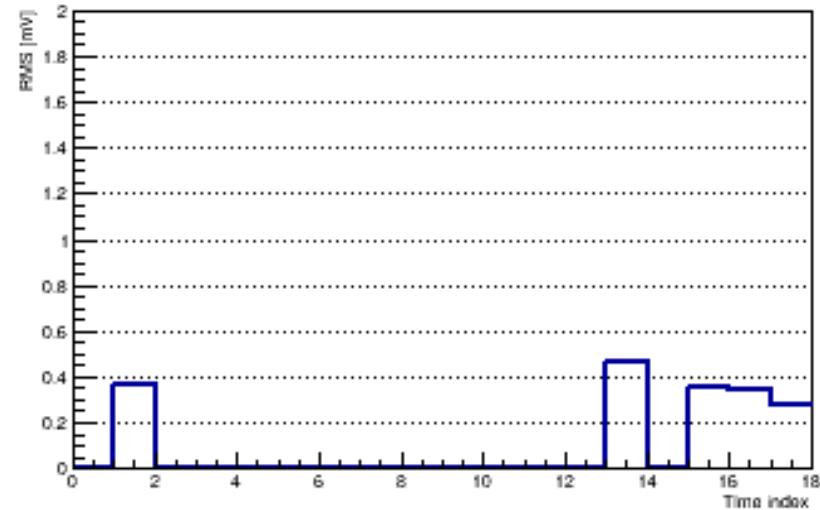


Time varying bins 41

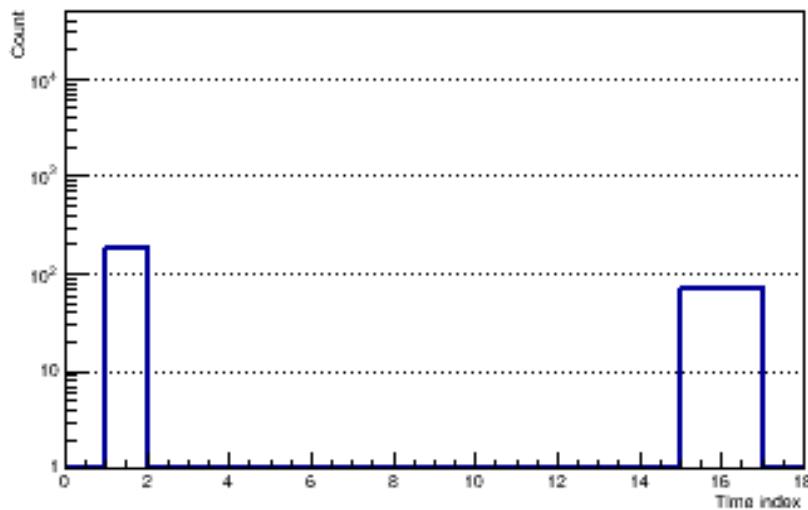
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 131



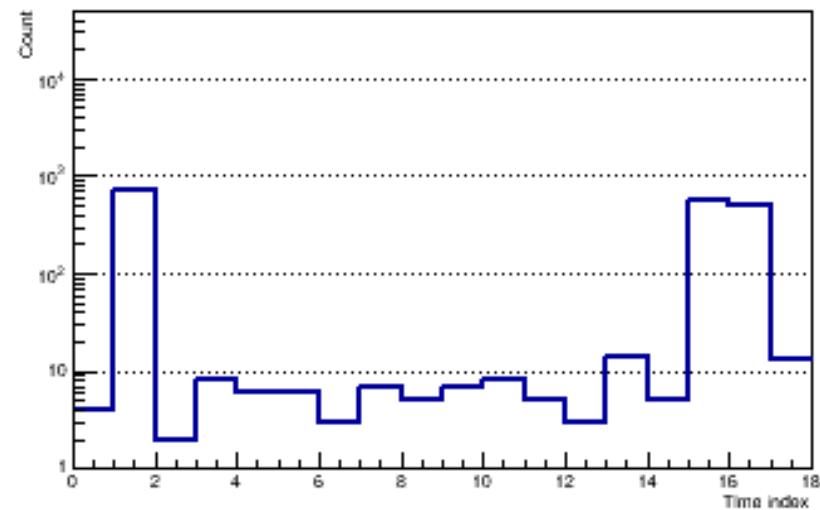
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 132



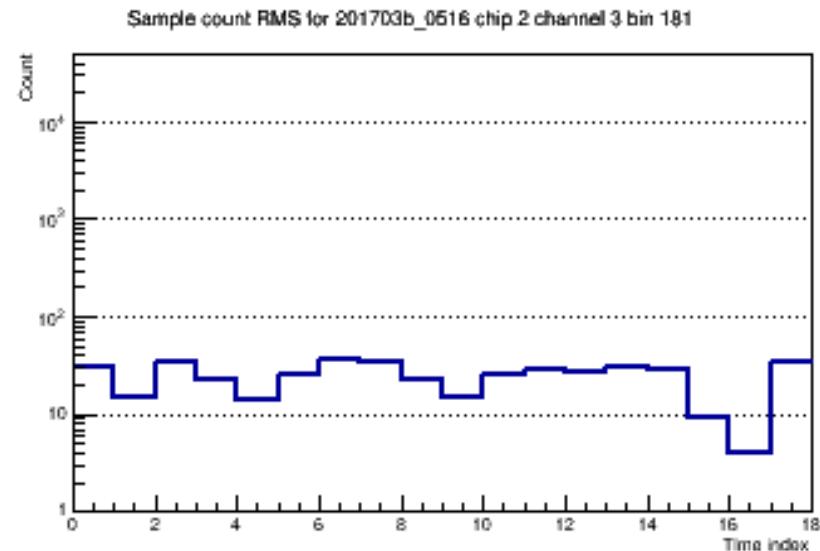
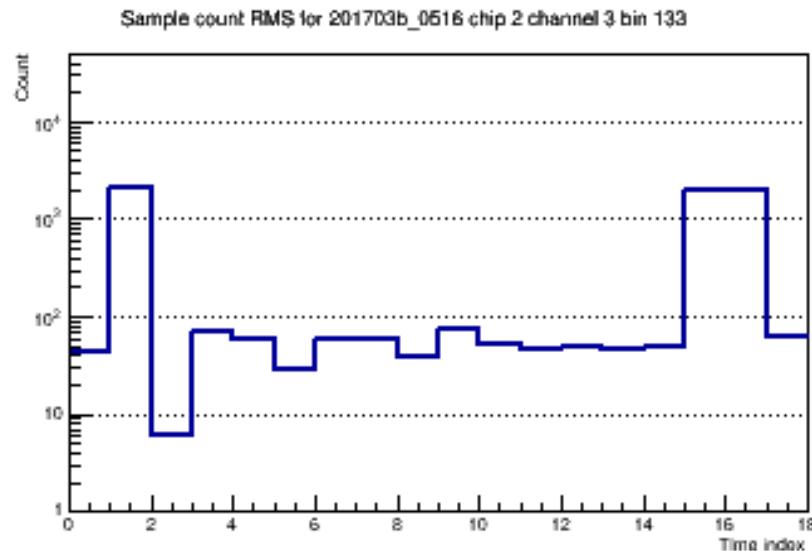
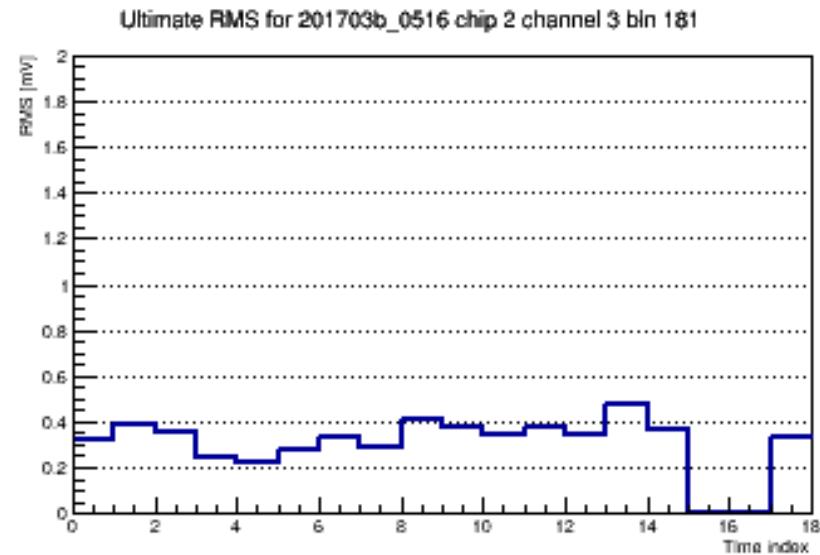
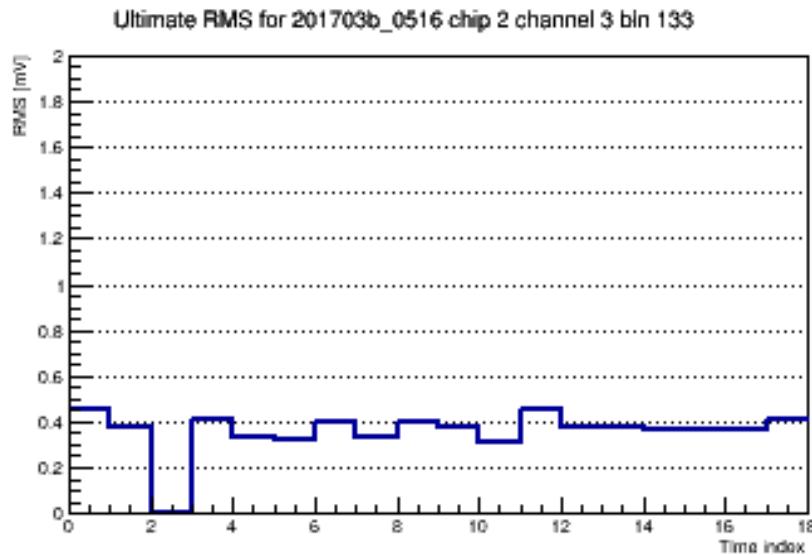
Sample count RMS for 201703b_0516 chip 2 channel 3 bin 131



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 132

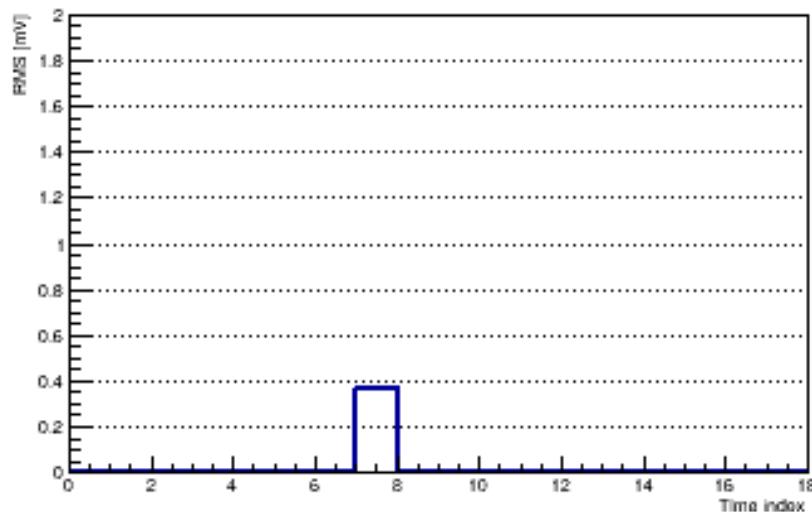


Time varying bins 42

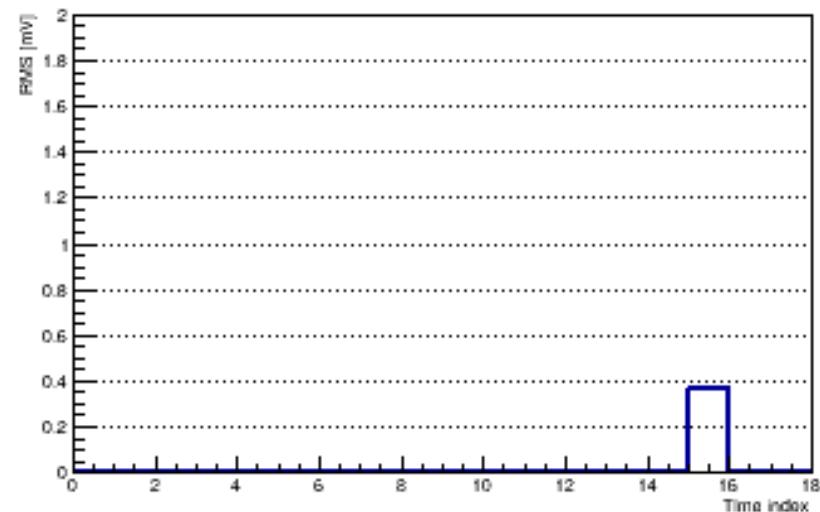


Time varying bins 43

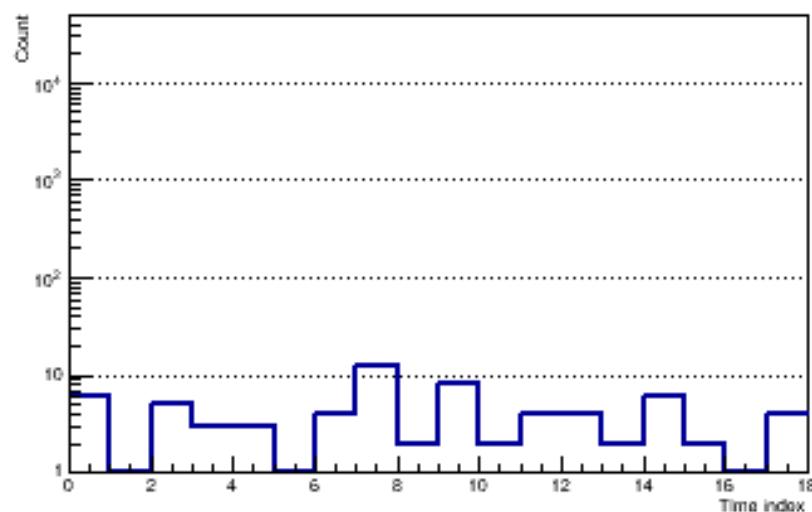
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 182



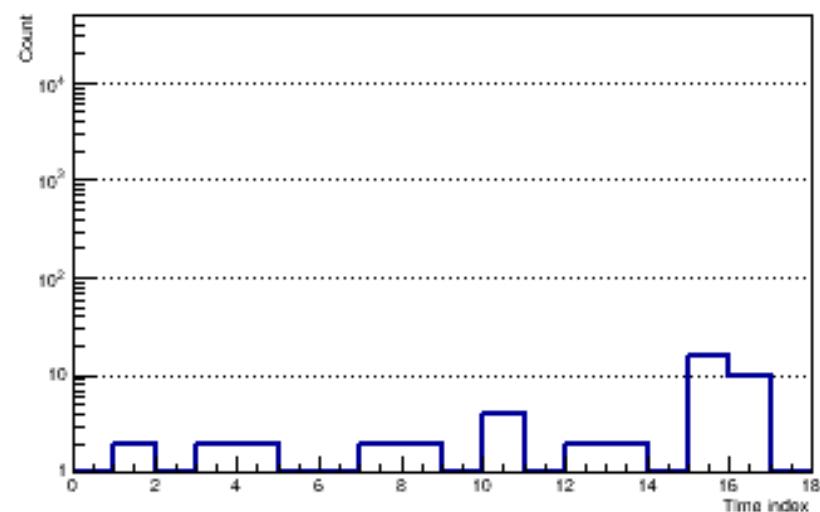
Ultimate RMS for 201703b_0516 chip 2 channel 3 bin 320



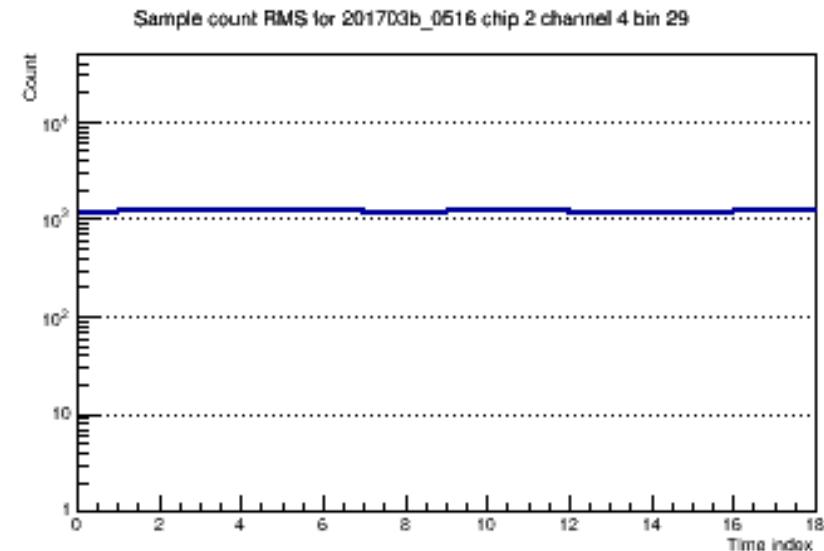
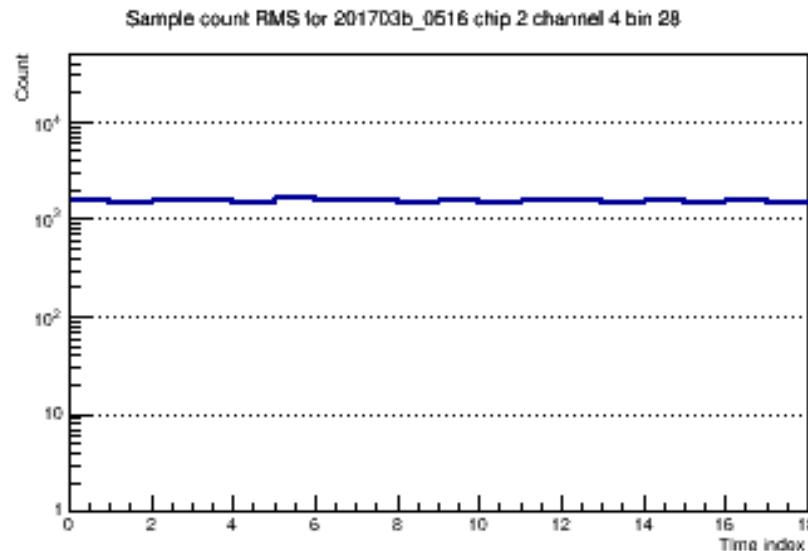
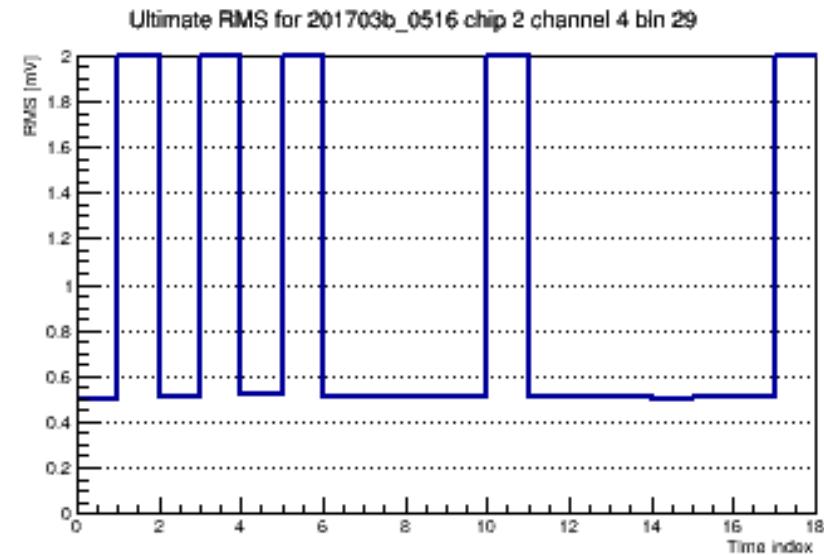
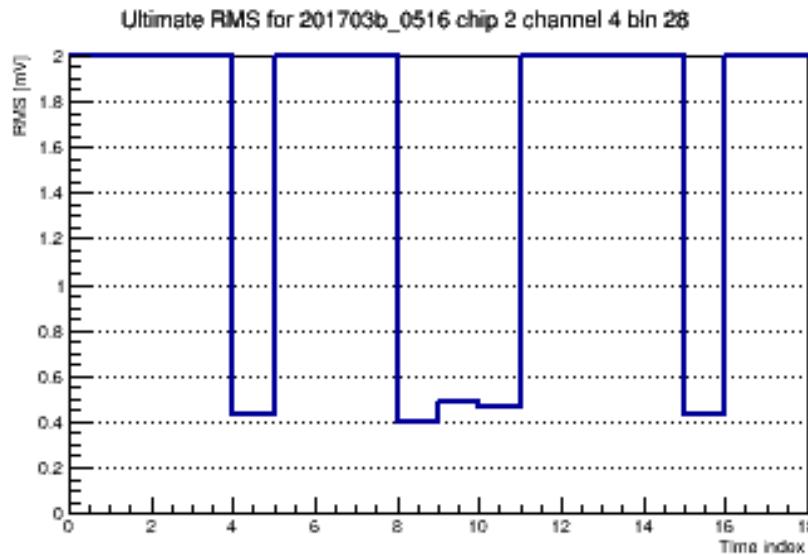
Sample count RMS for 201703b_0516 chip 2 channel 3 bin 182



Sample count RMS for 201703b_0516 chip 2 channel 3 bin 320

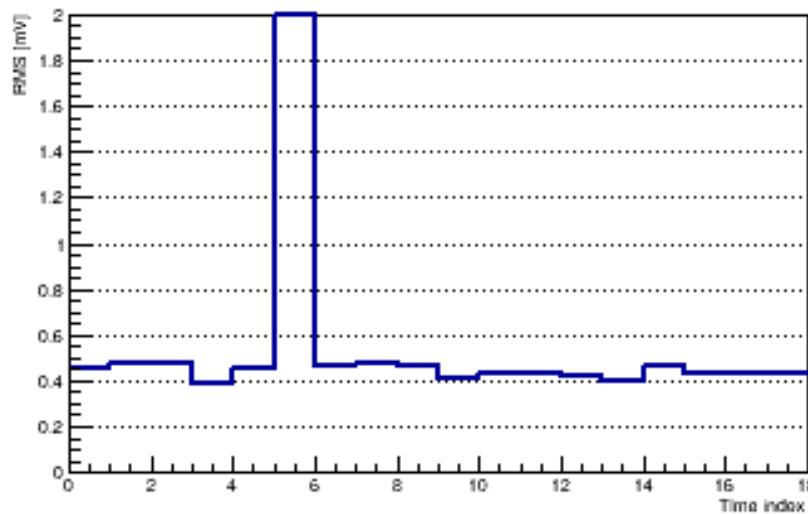


Time varying bins 44

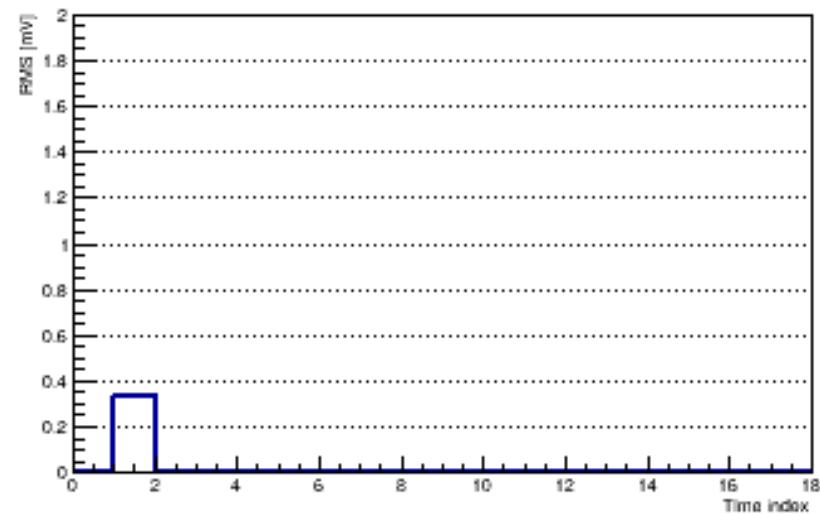


Time varying bins 45

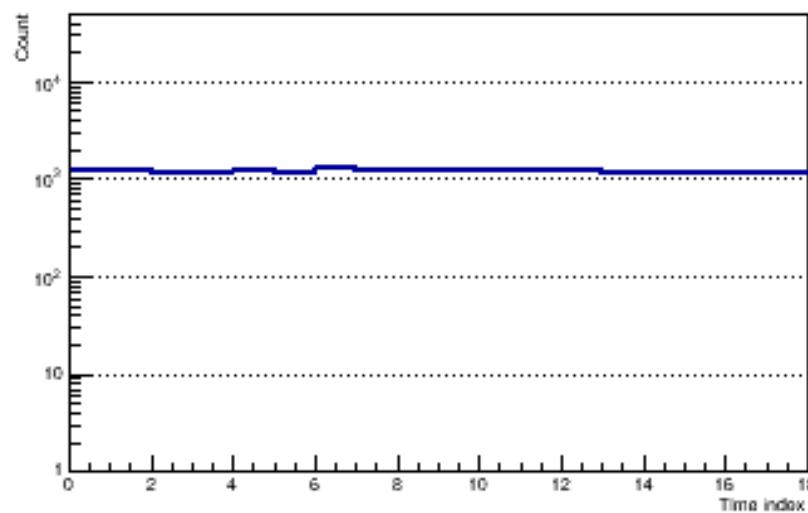
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 30



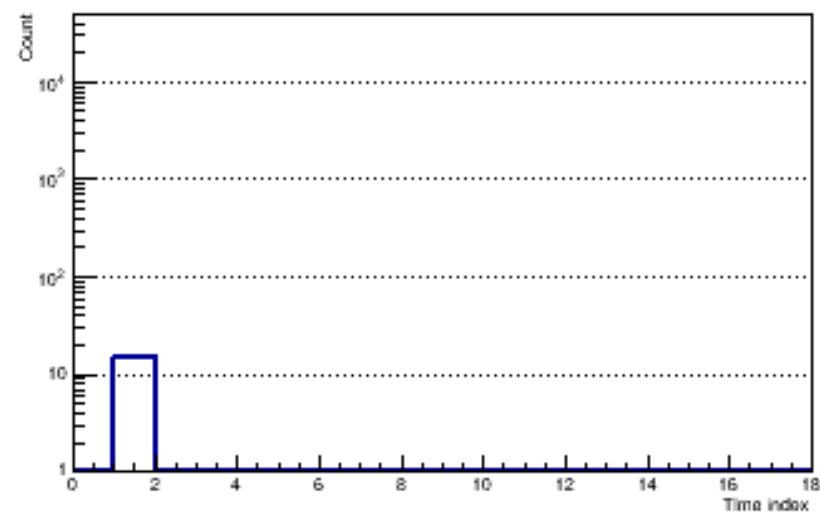
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 105



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 30

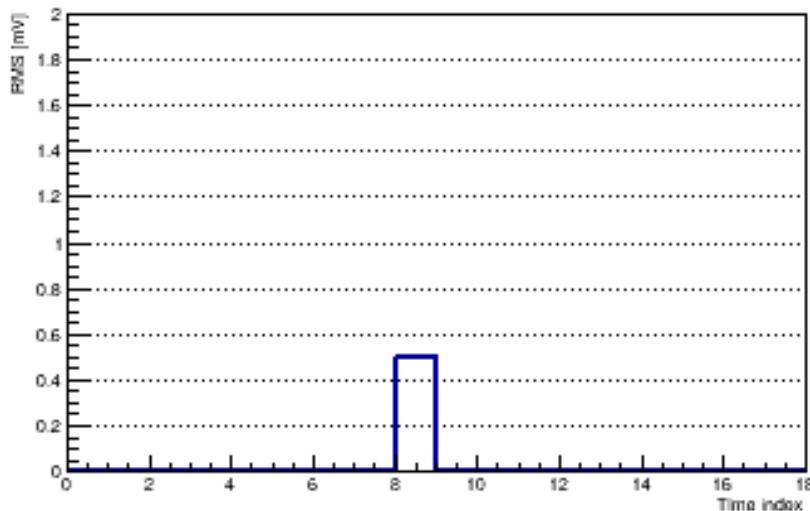


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 105

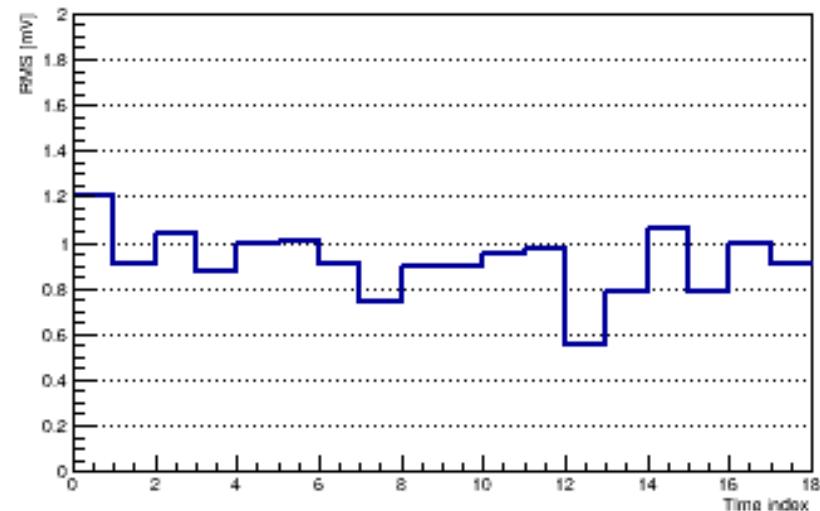


Time varying bins 46

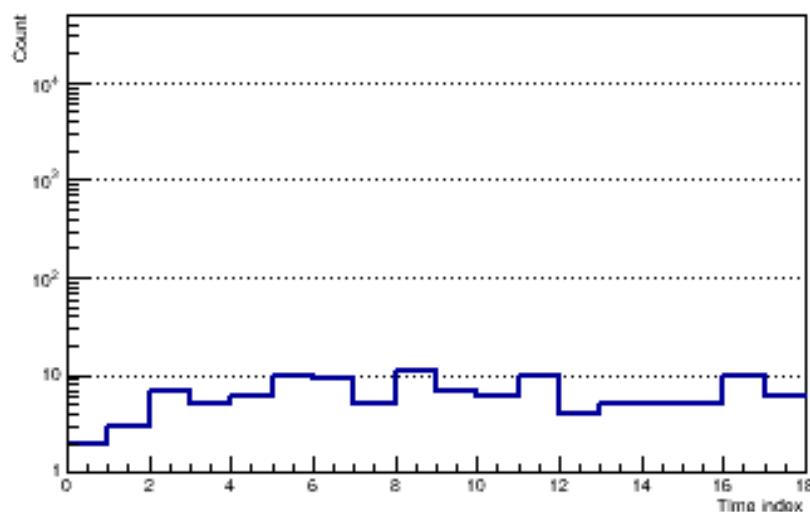
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 1152



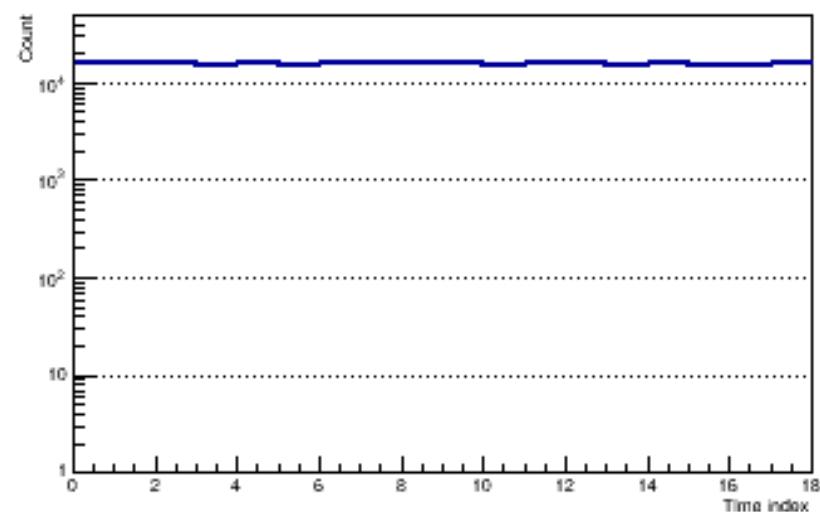
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 1215



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 1152

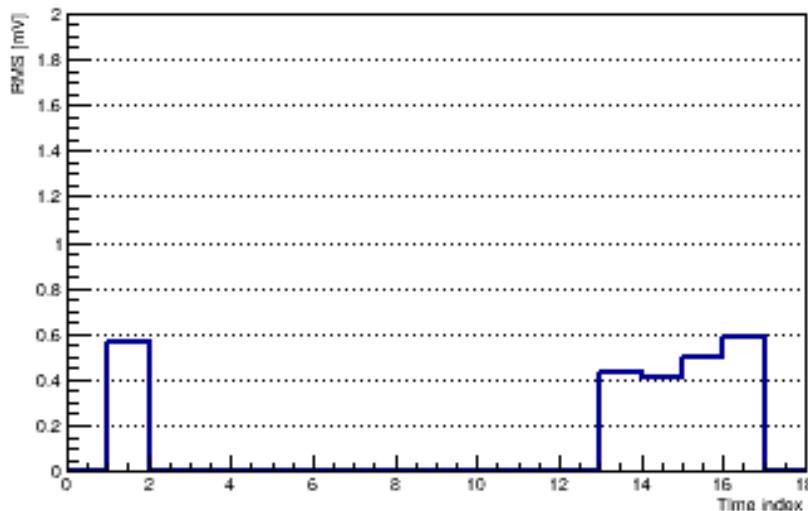


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 1215

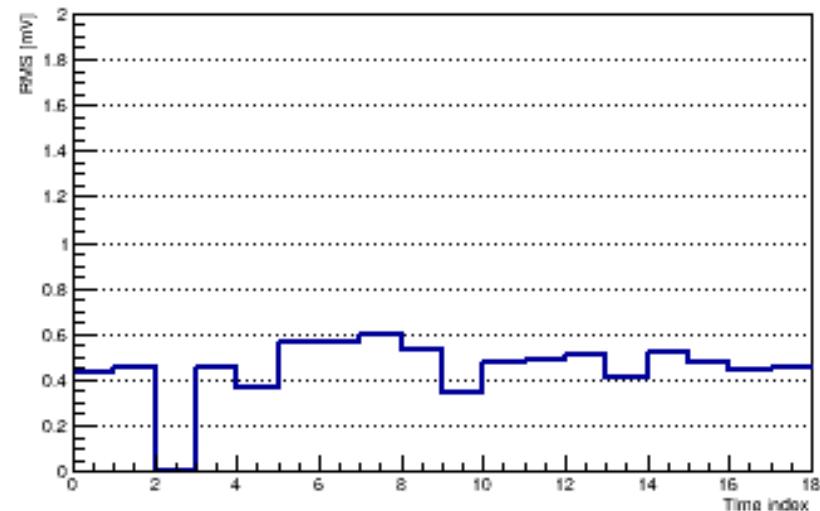


Time varying bins 47

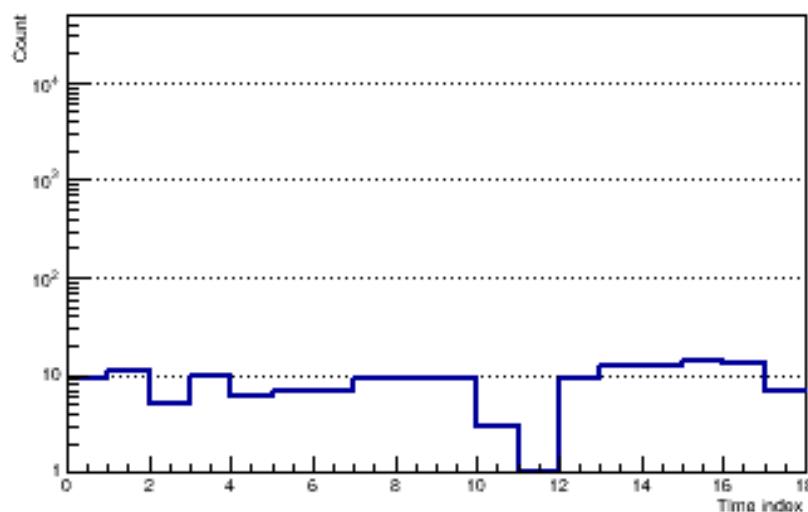
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 1280



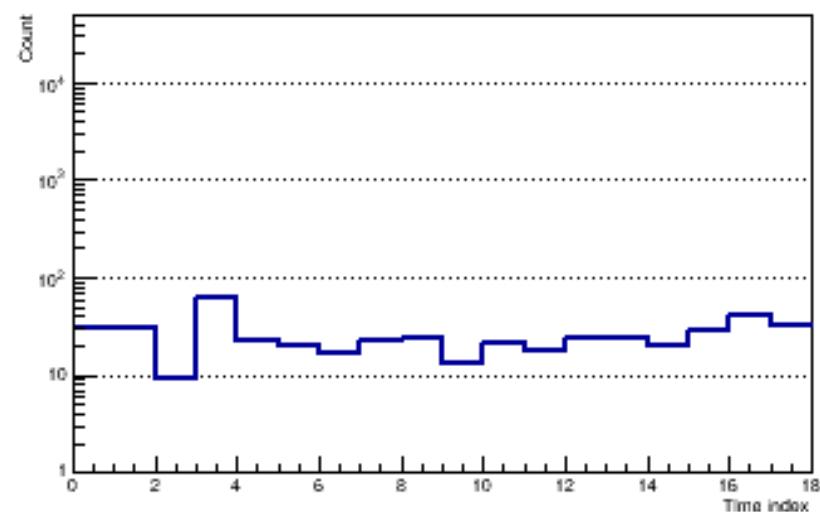
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 1344



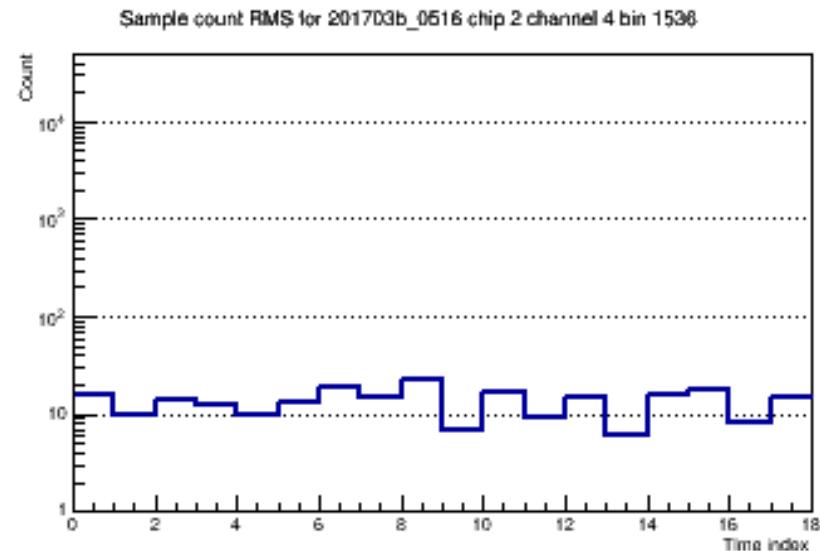
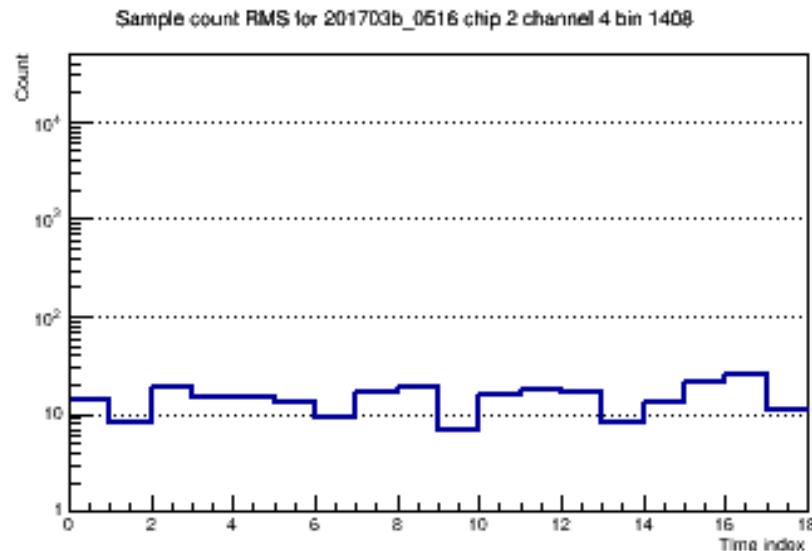
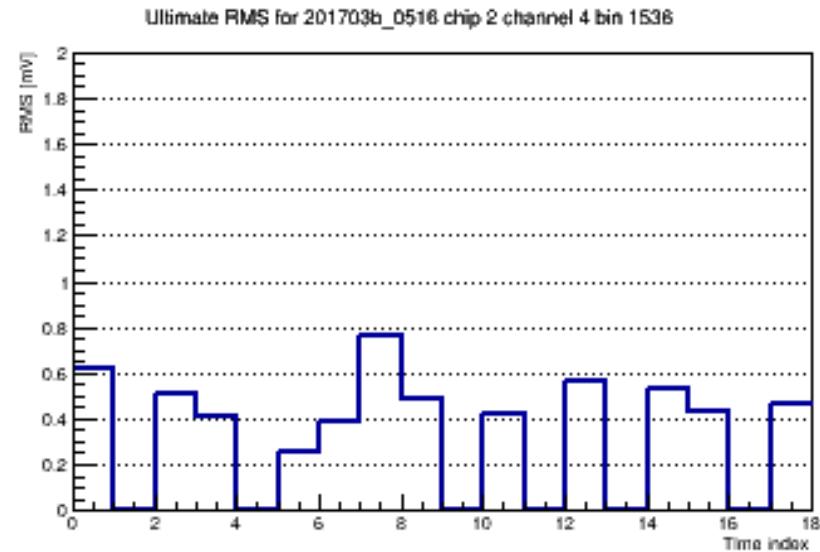
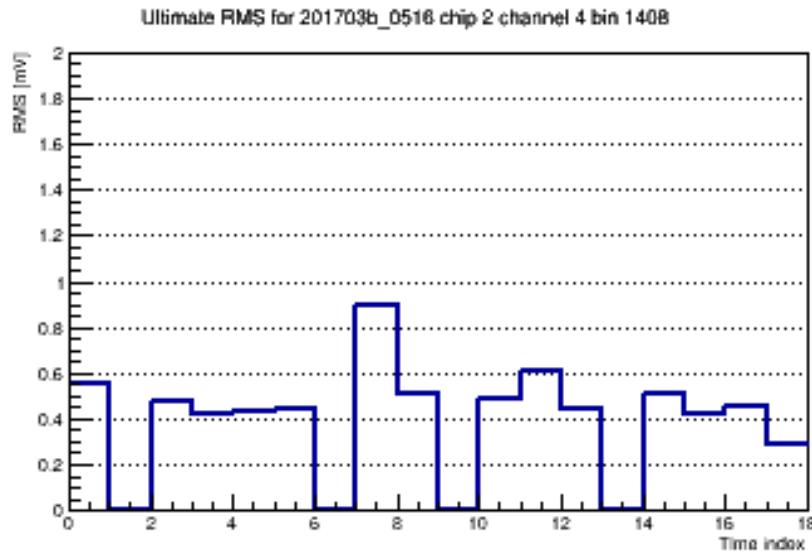
Sample count RMS for 201703b_0516 chip 2 channel 4 bin 1280



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 1344

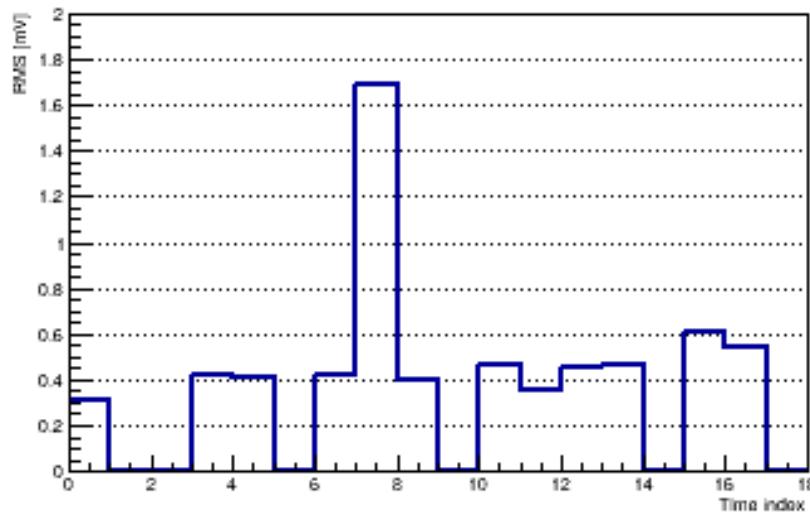


Time varying bins 48

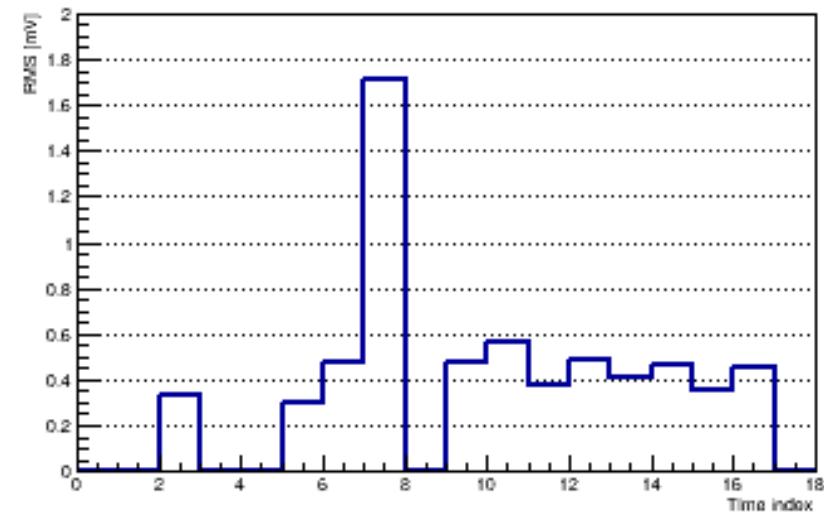


Time varying bins 49

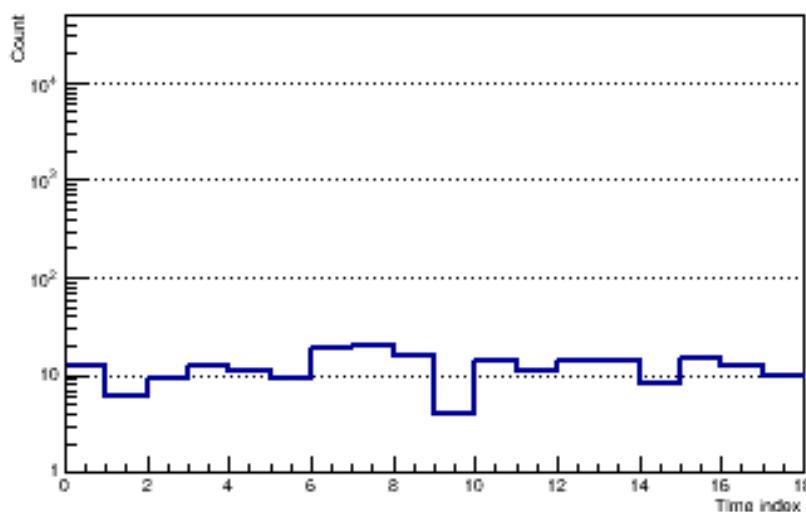
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 1664



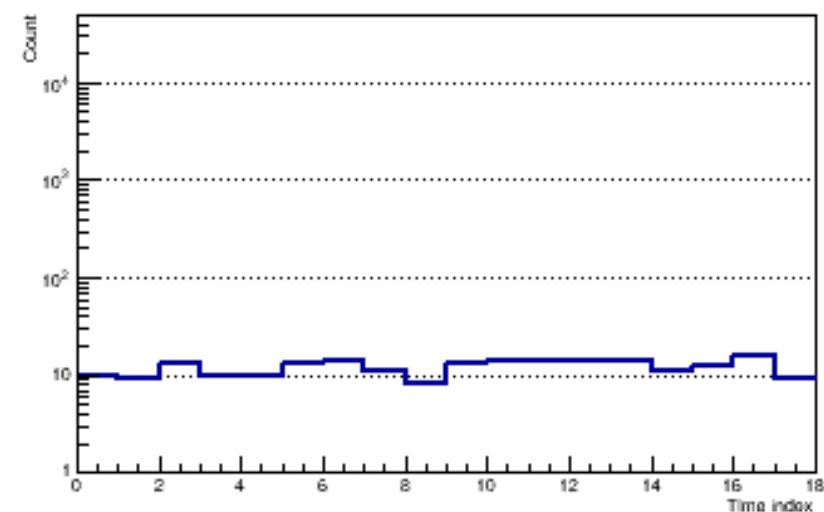
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 1728



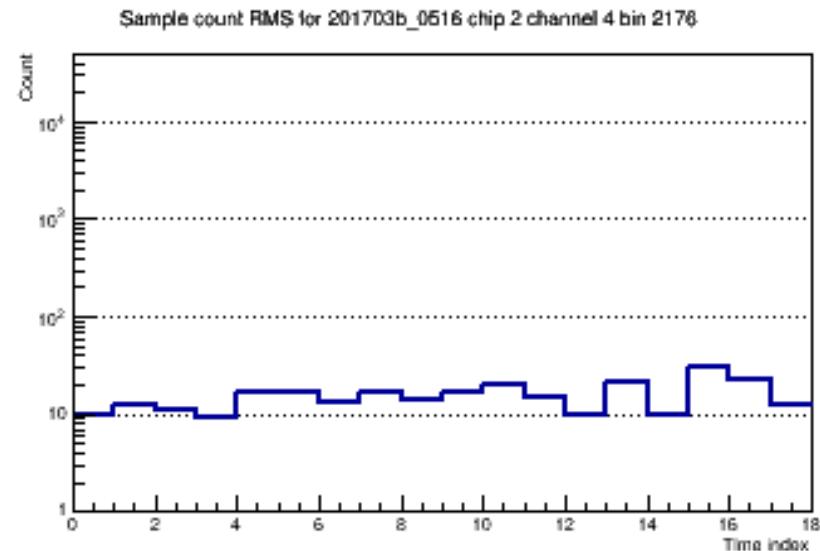
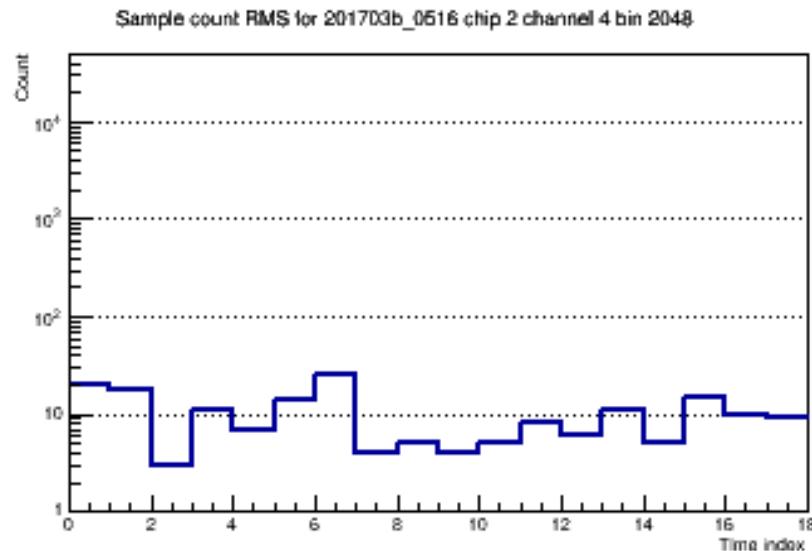
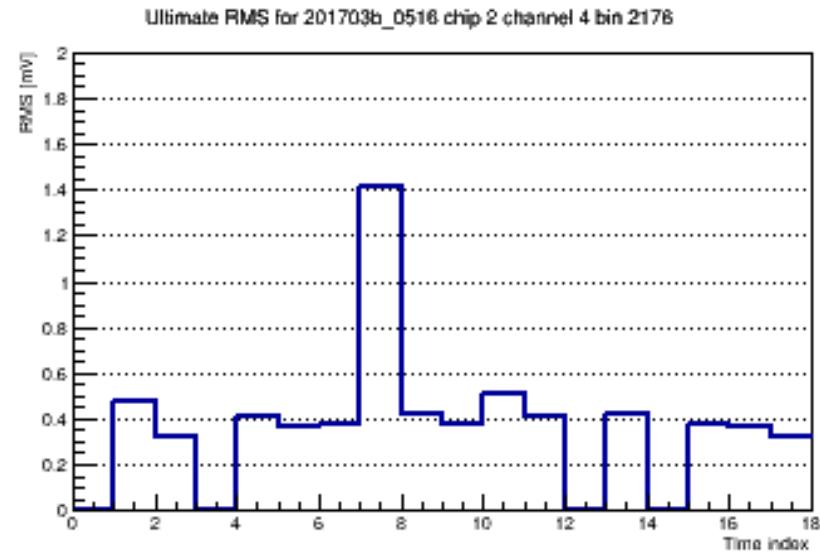
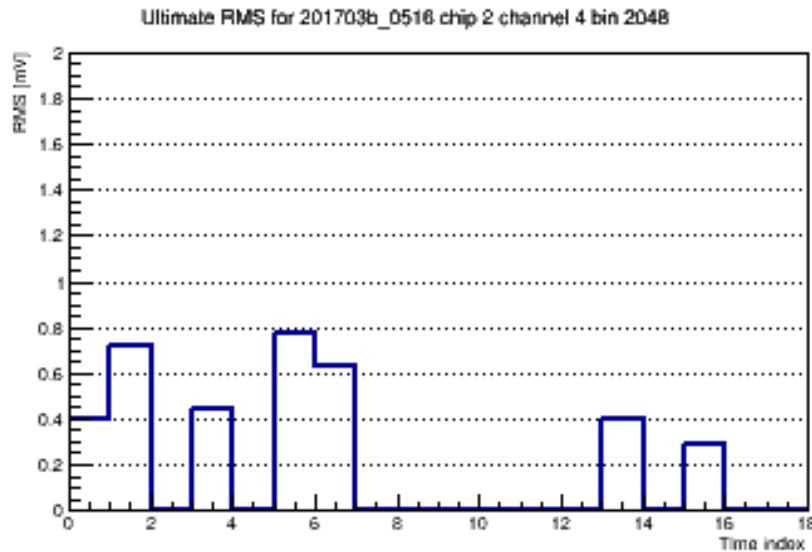
Sample count RMS for 201703b_0516 chip 2 channel 4 bin 1664



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 1728

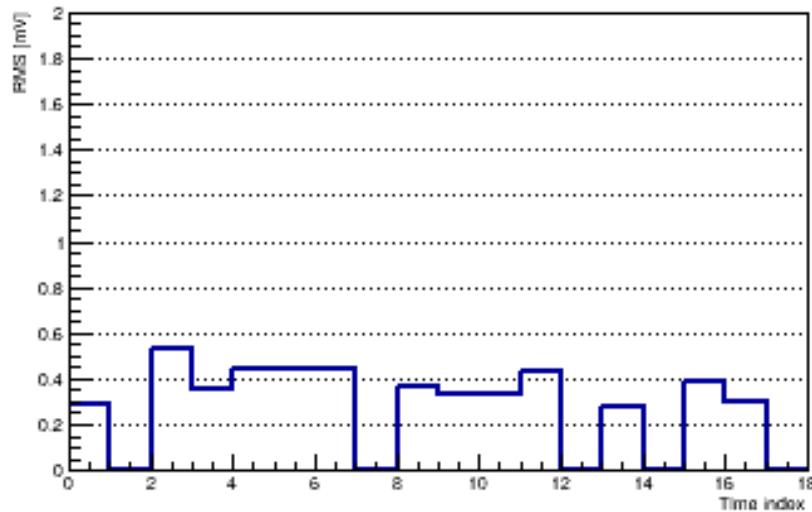


Time varying bins 50

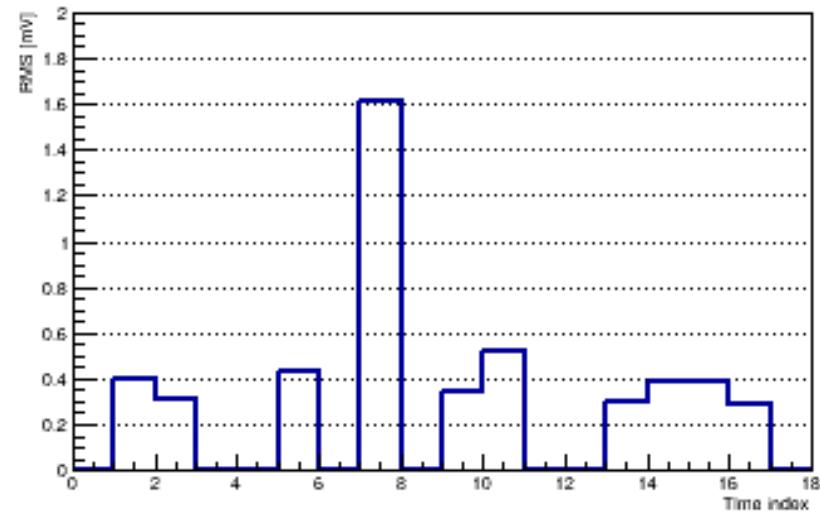


Time varying bins 51

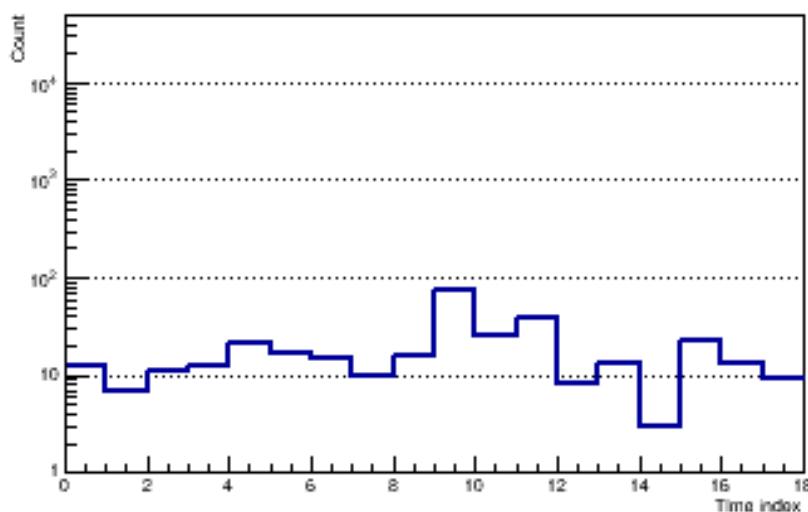
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 2240



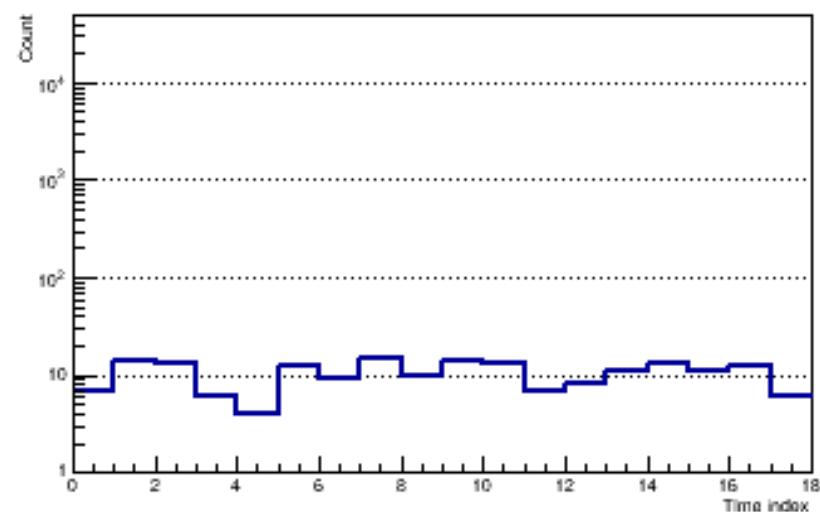
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 2368



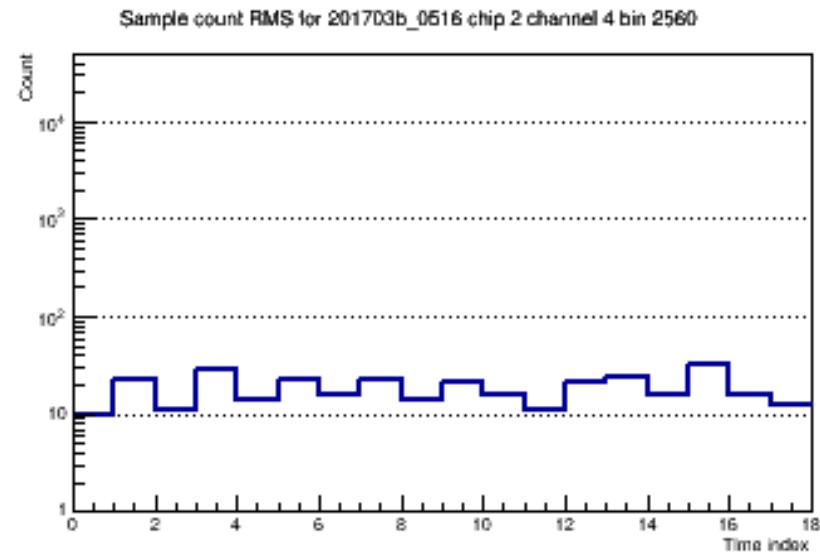
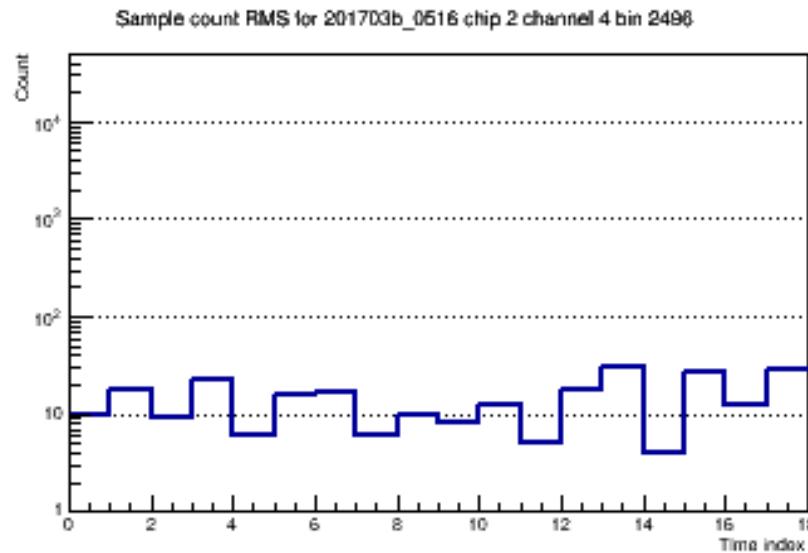
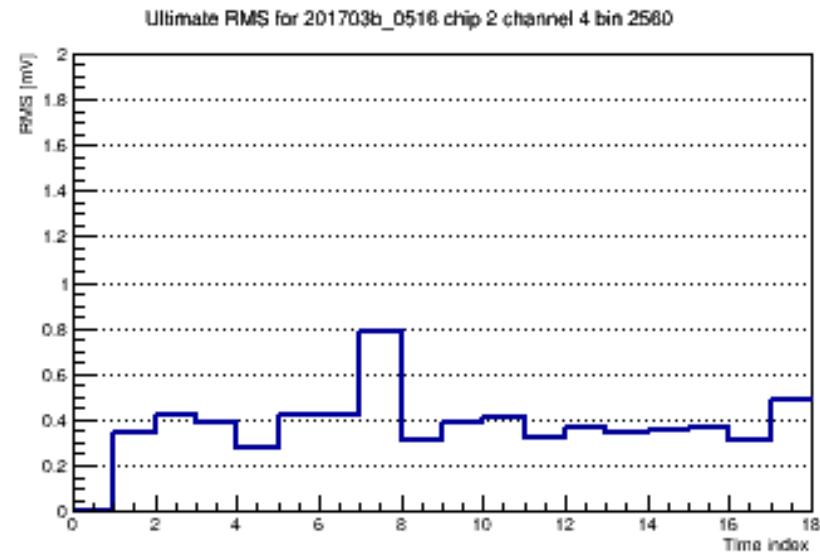
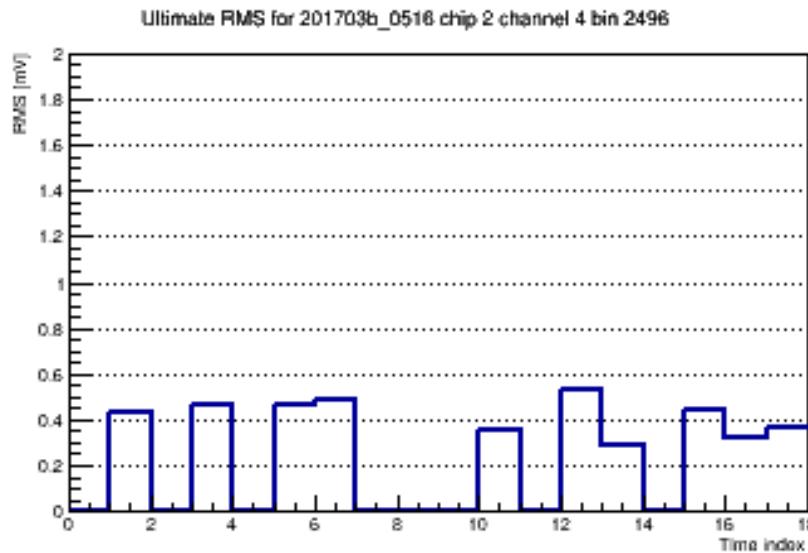
Sample count RMS for 201703b_0516 chip 2 channel 4 bin 2240



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 2368

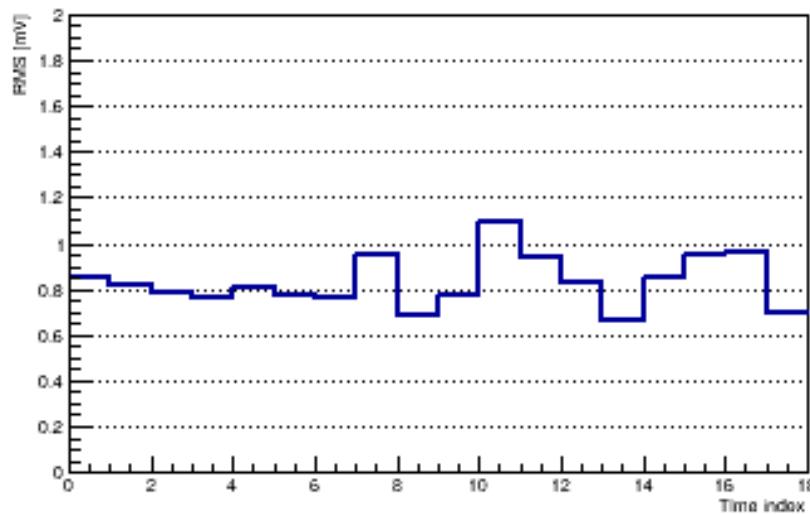


Time varying bins 52

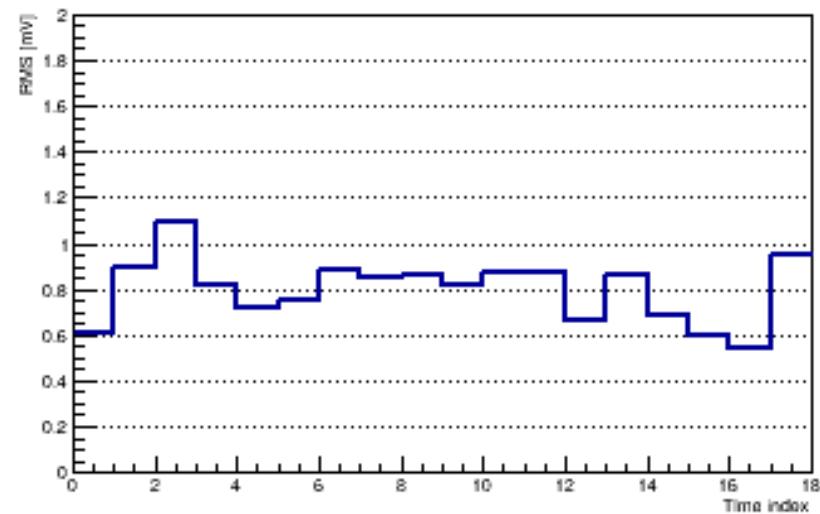


Time varying bins 53

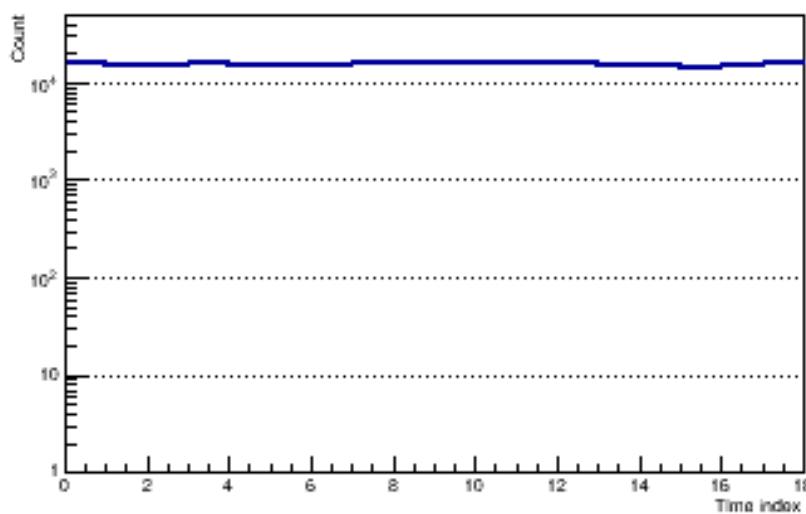
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 3071



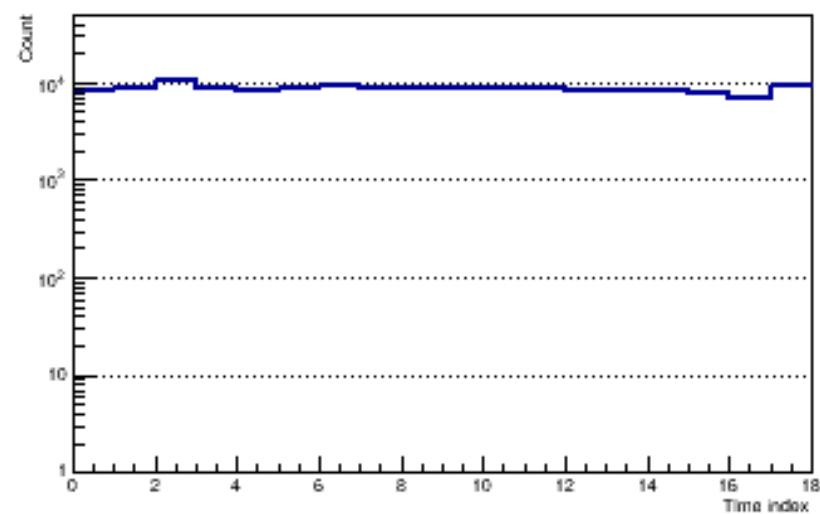
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 4089



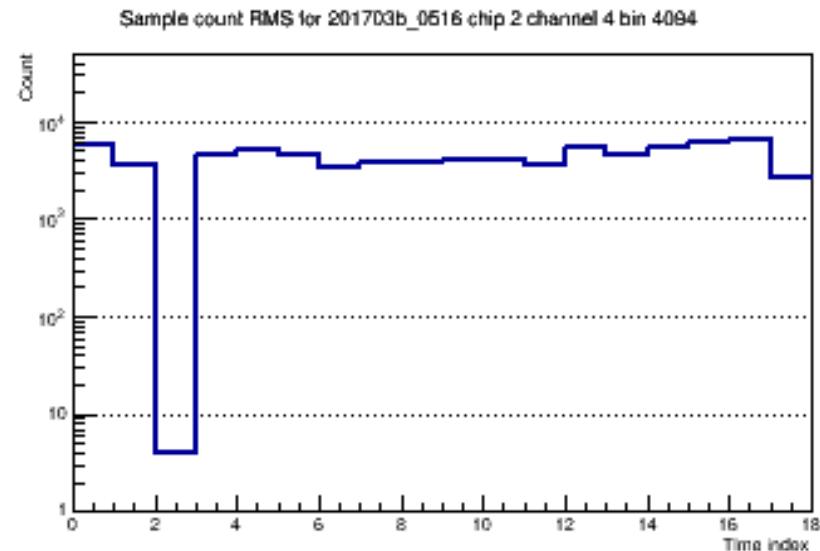
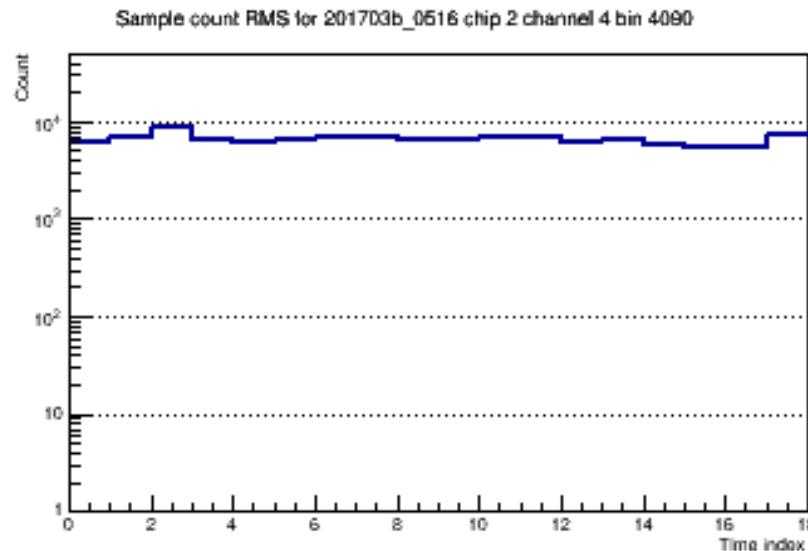
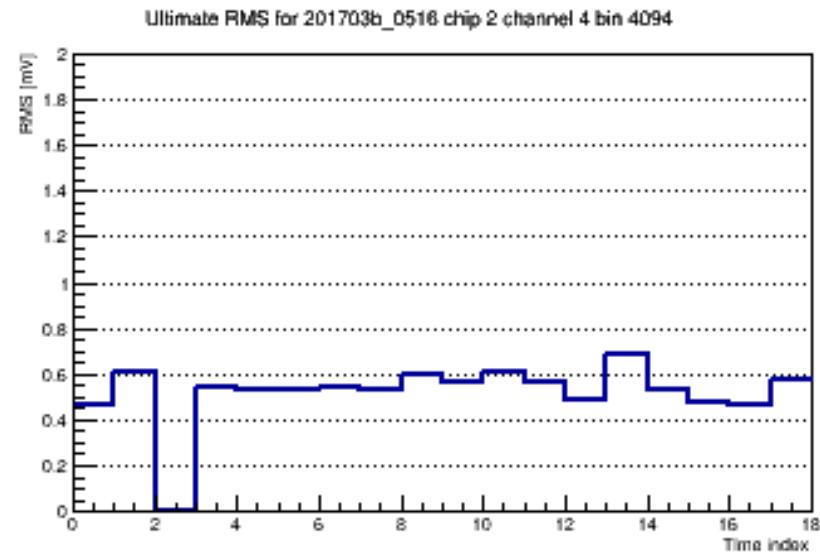
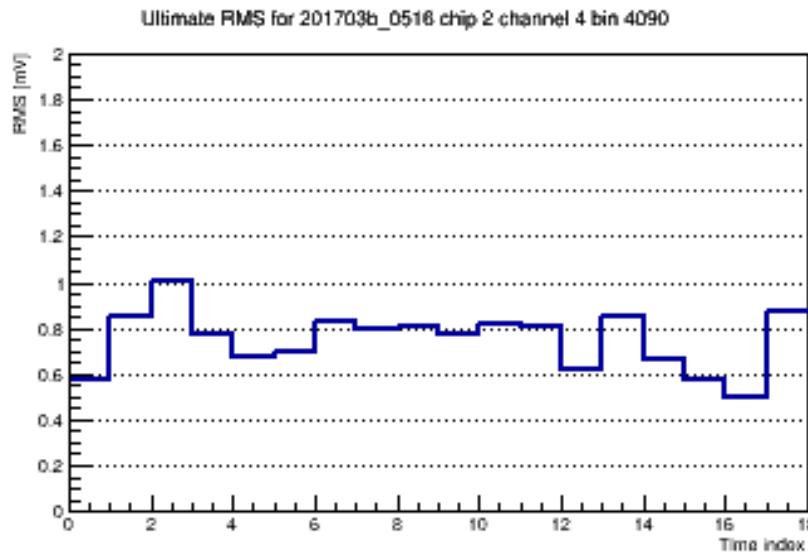
Sample count RMS for 201703b_0516 chip 2 channel 4 bin 3071



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 4089

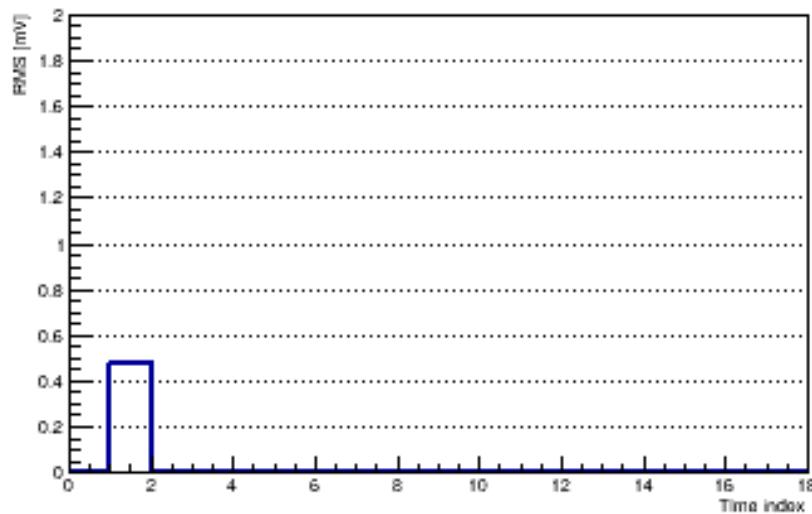


Time varying bins 54

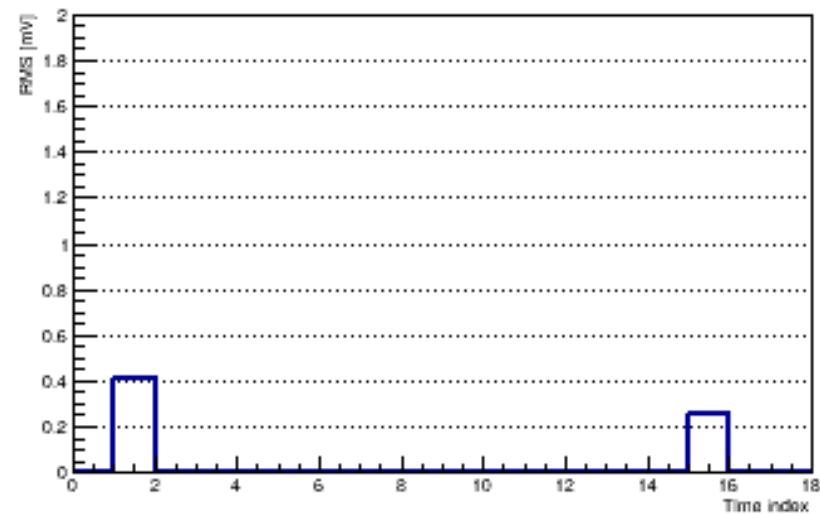


Time varying bins 55

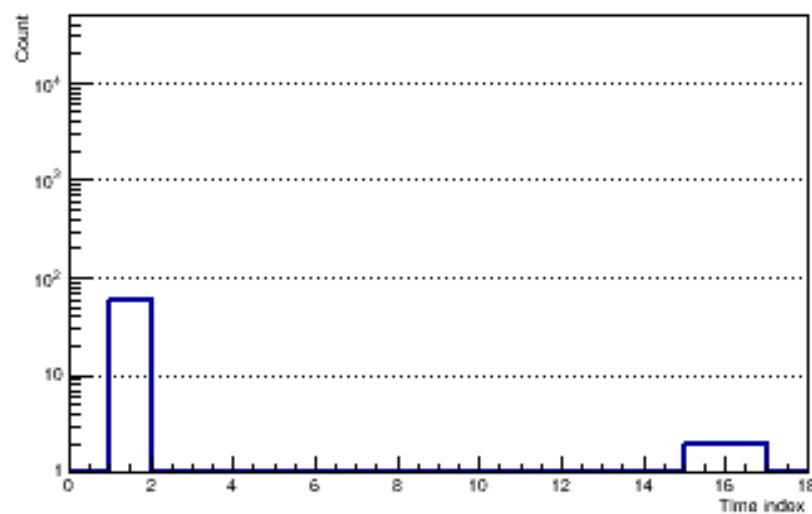
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 106



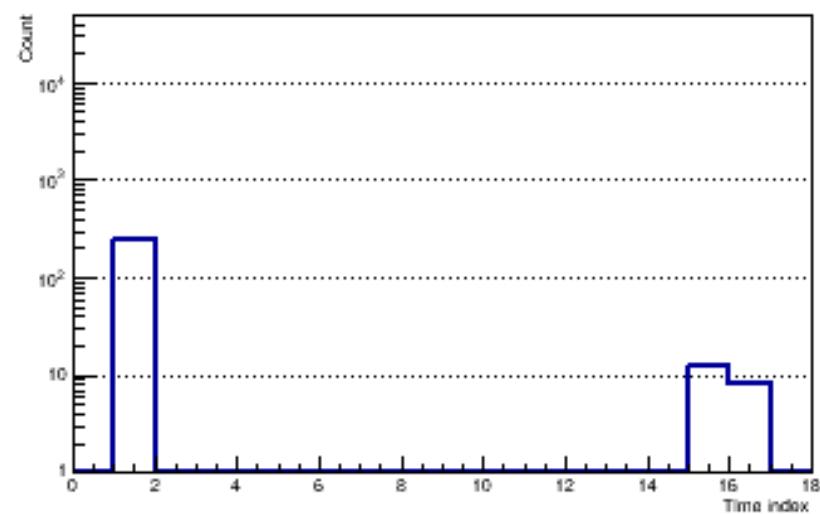
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 107



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 106

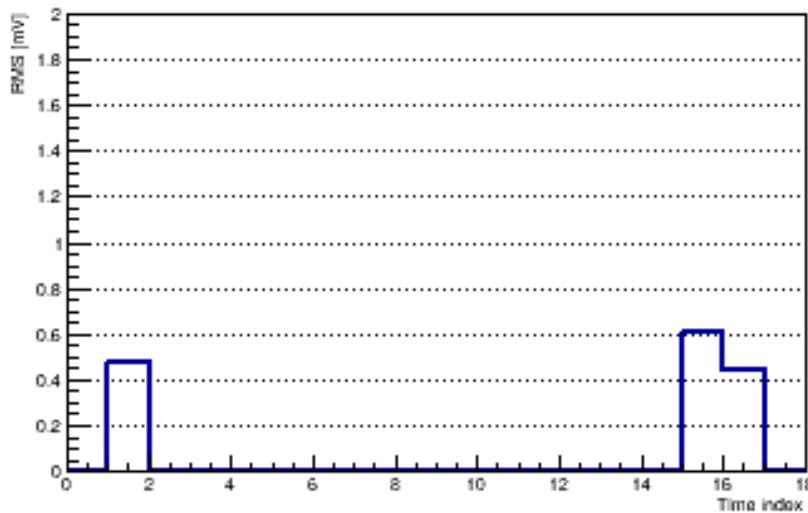


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 107

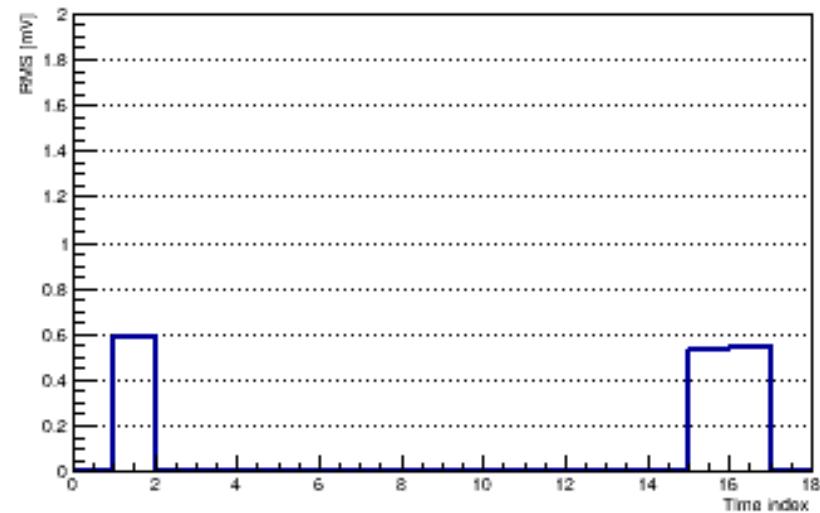


Time varying bins 56

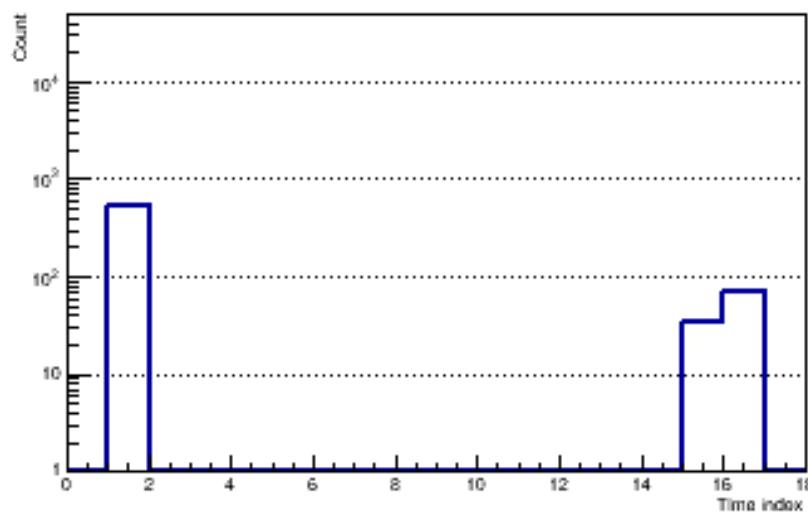
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 108



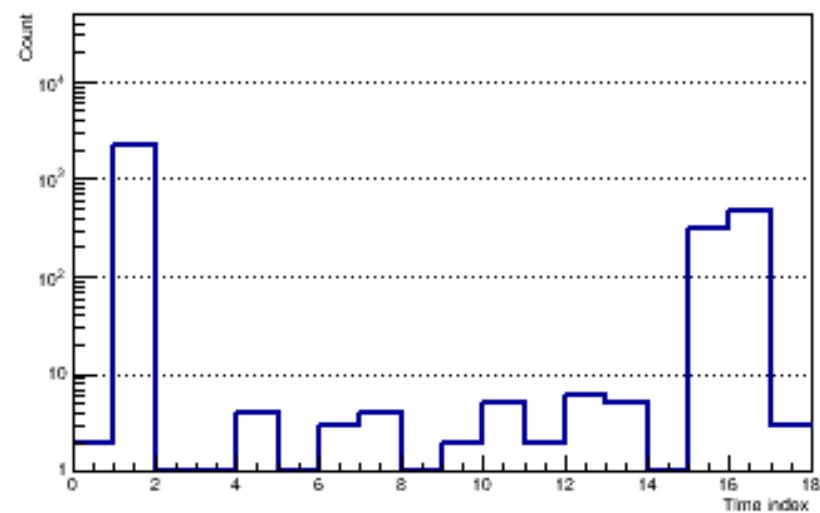
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 109



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 108

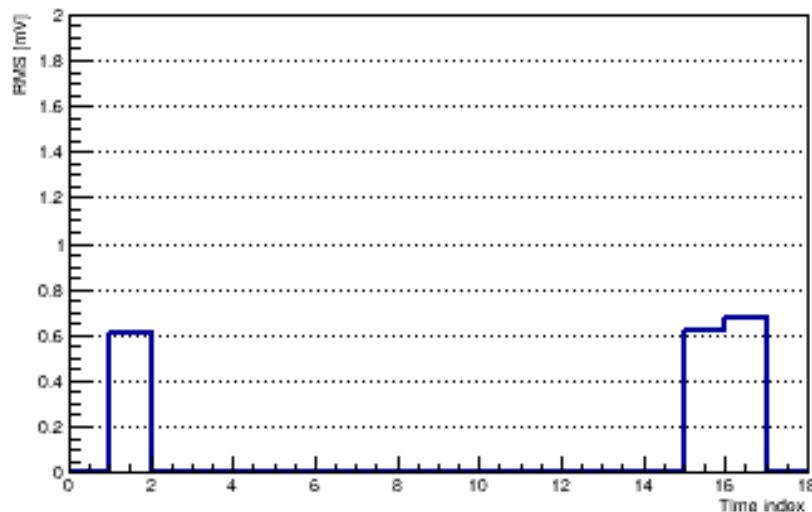


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 109

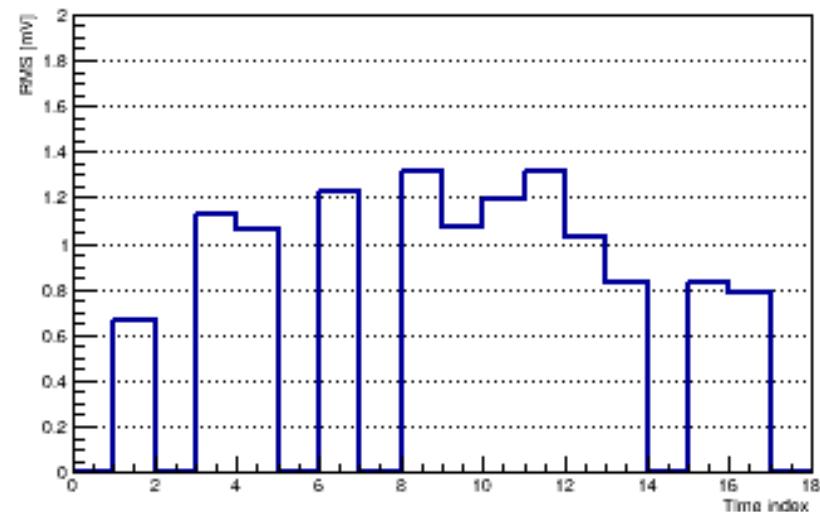


Time varying bins 57

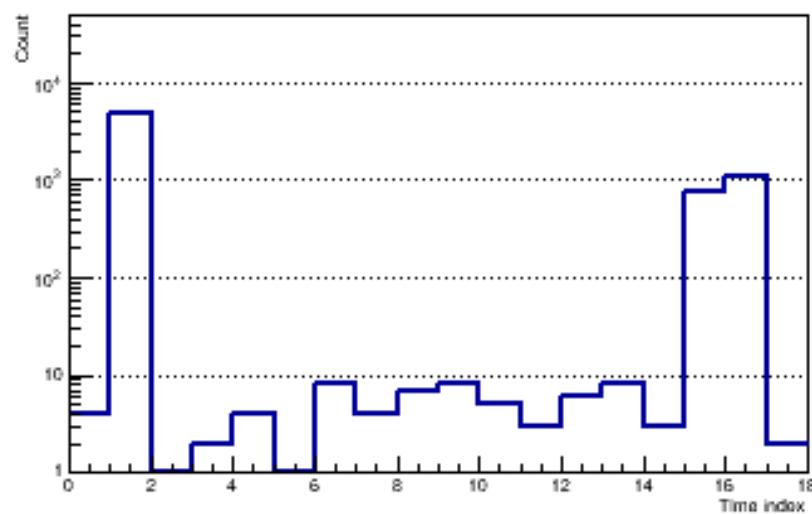
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 110



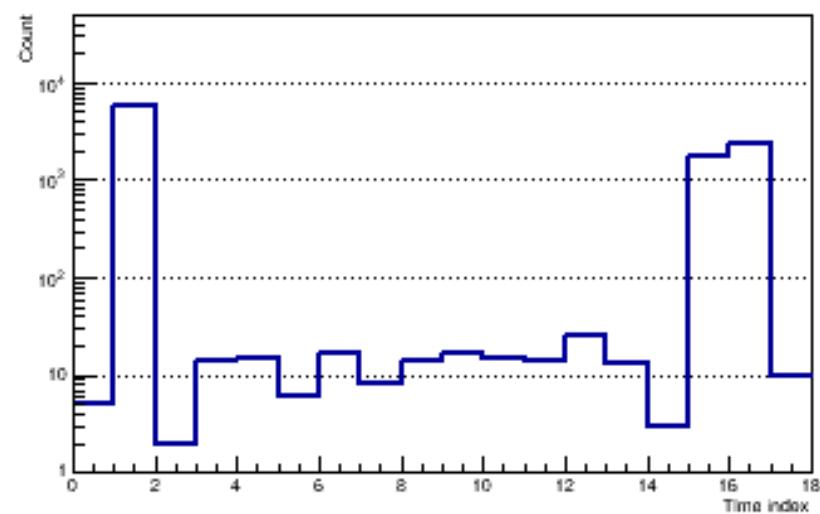
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 111



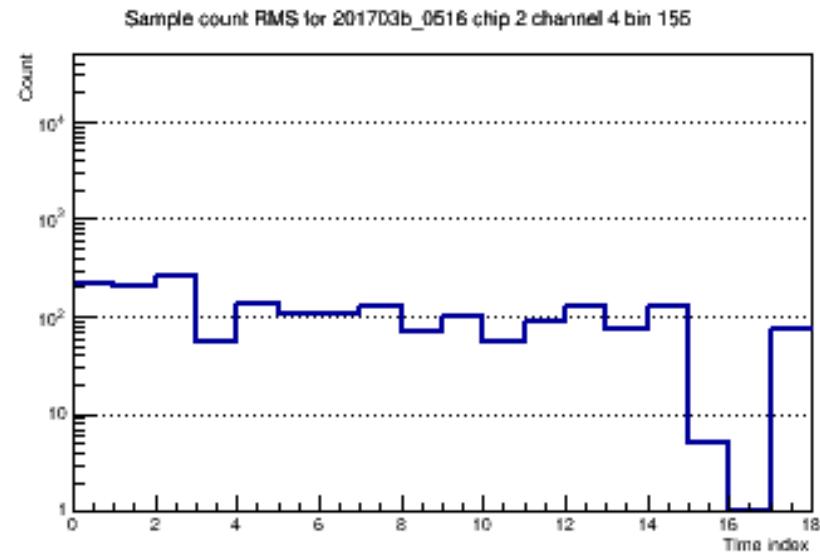
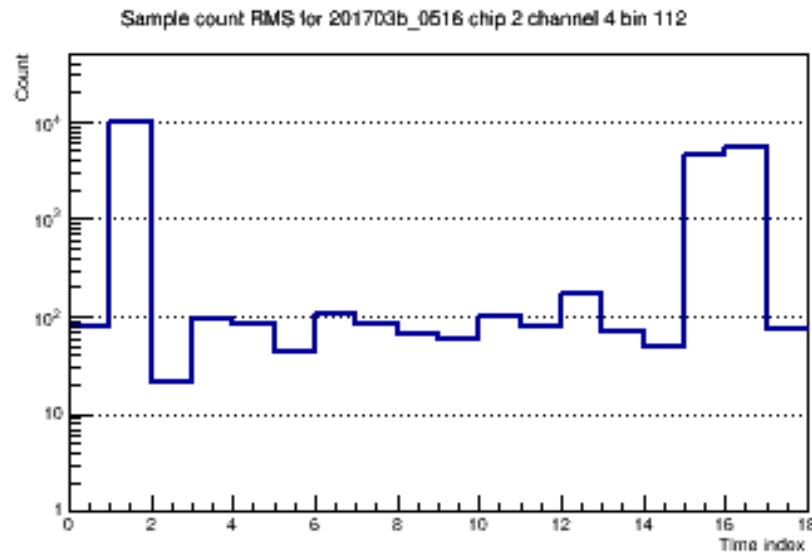
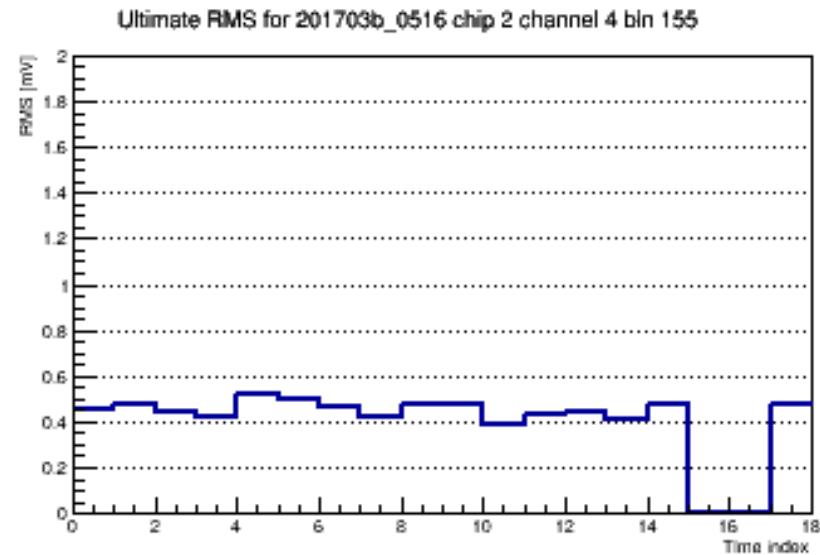
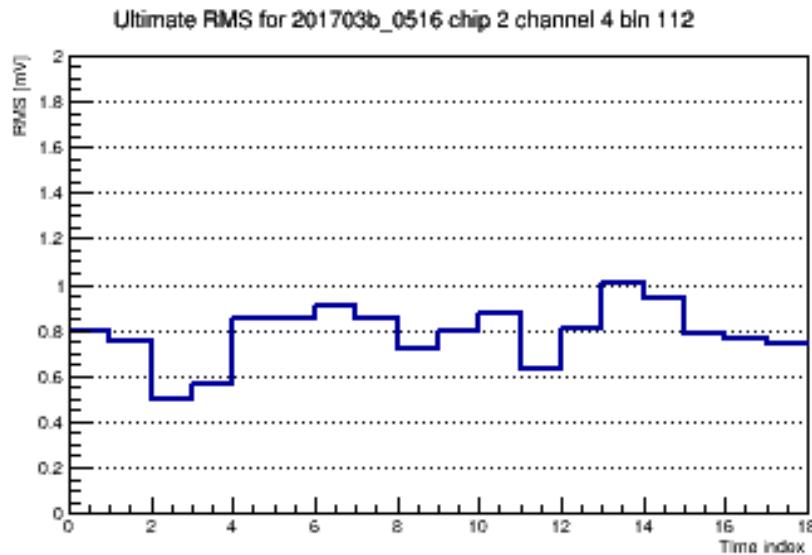
Sample count RMS for 201703b_0516 chip 2 channel 4 bin 110



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 111

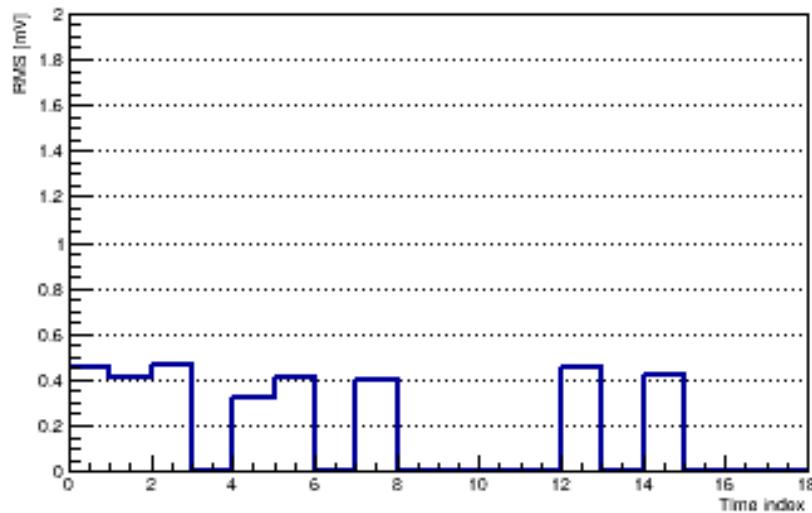


Time varying bins 58

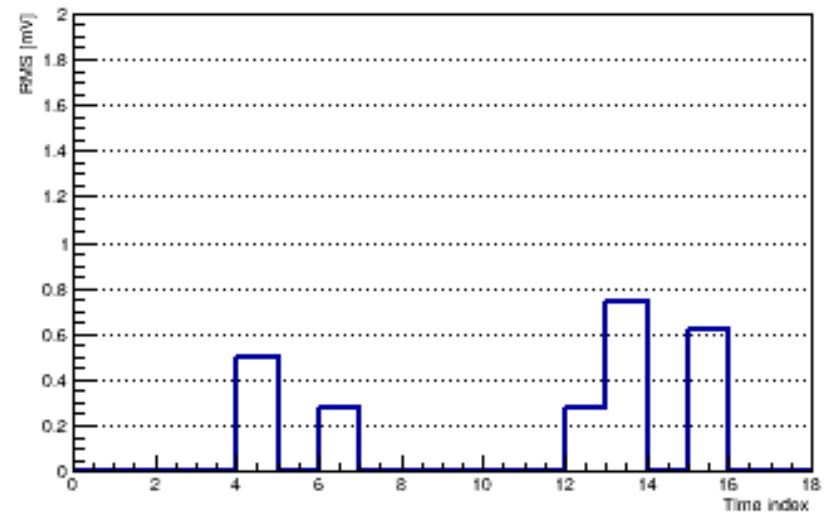


Time varying bins 59

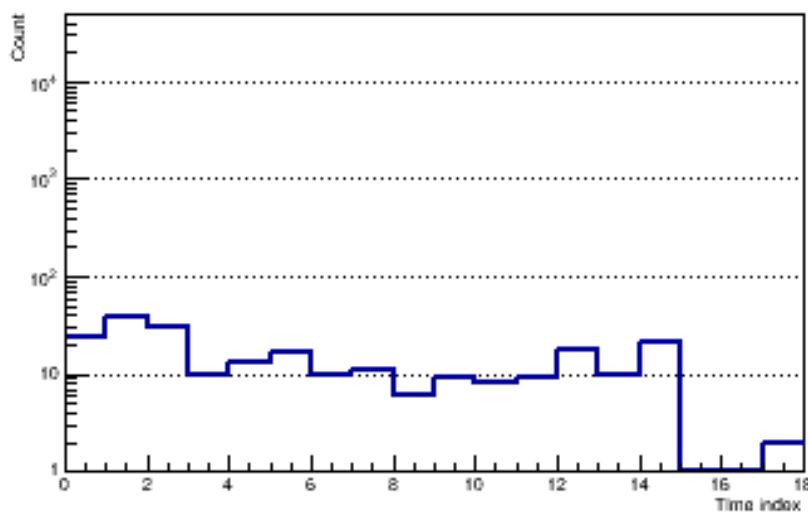
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 156



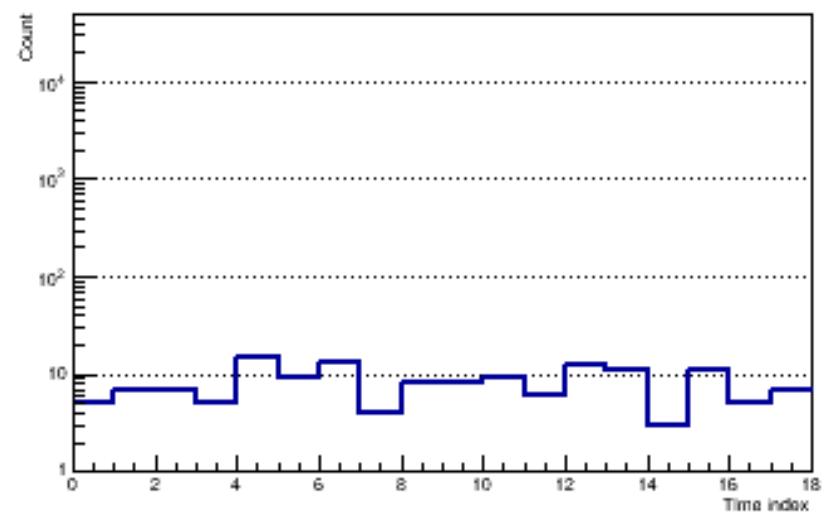
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 283



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 156

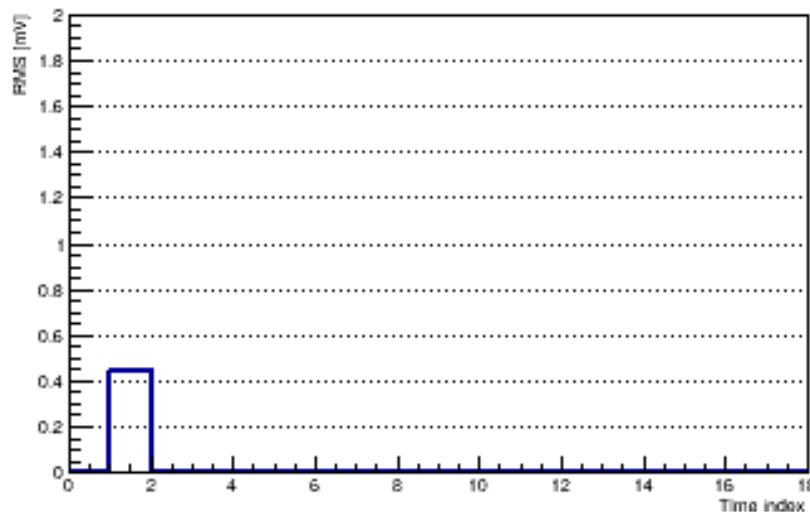


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 283

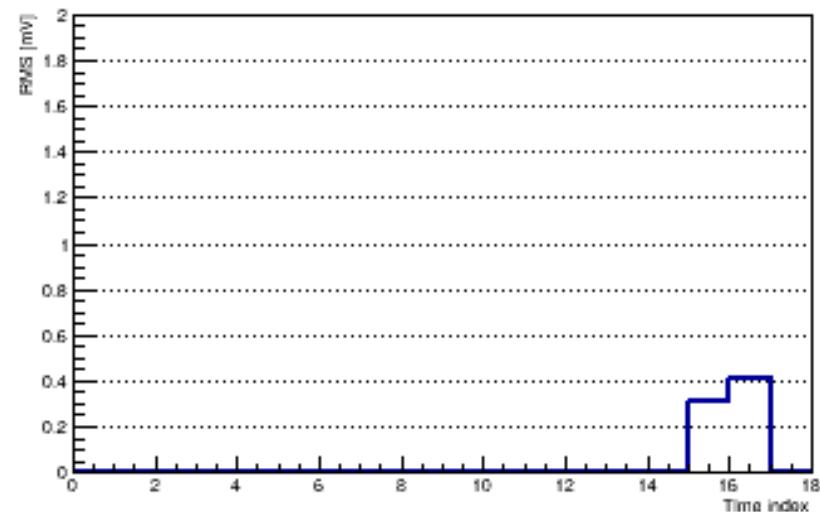


Time varying bins 60

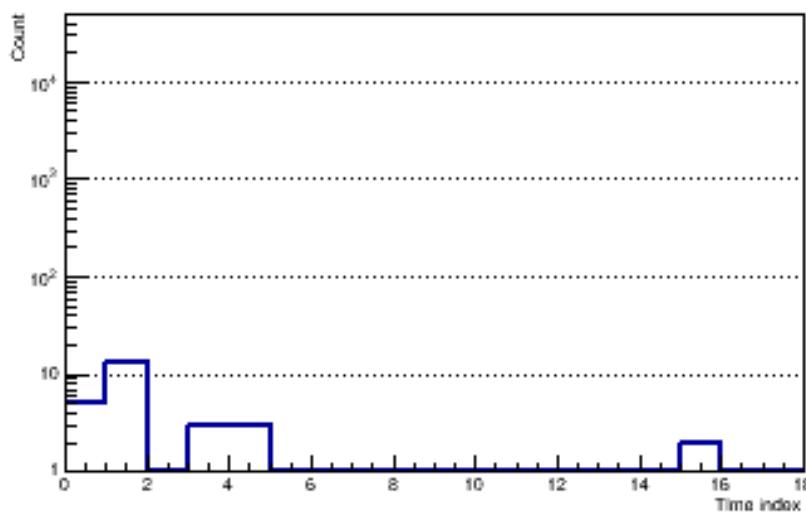
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 328



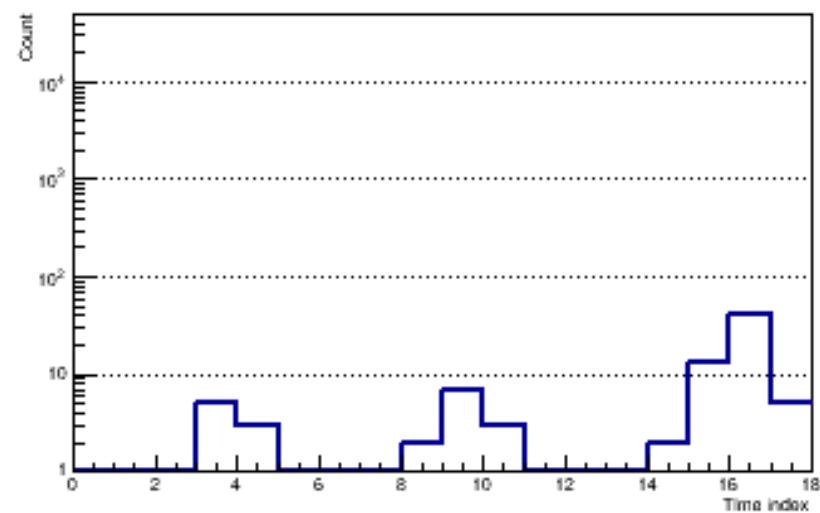
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 330



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 328

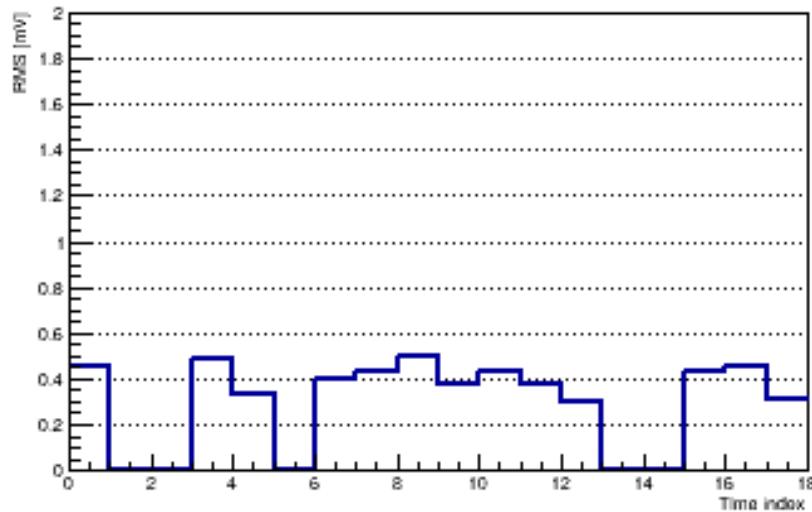


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 330

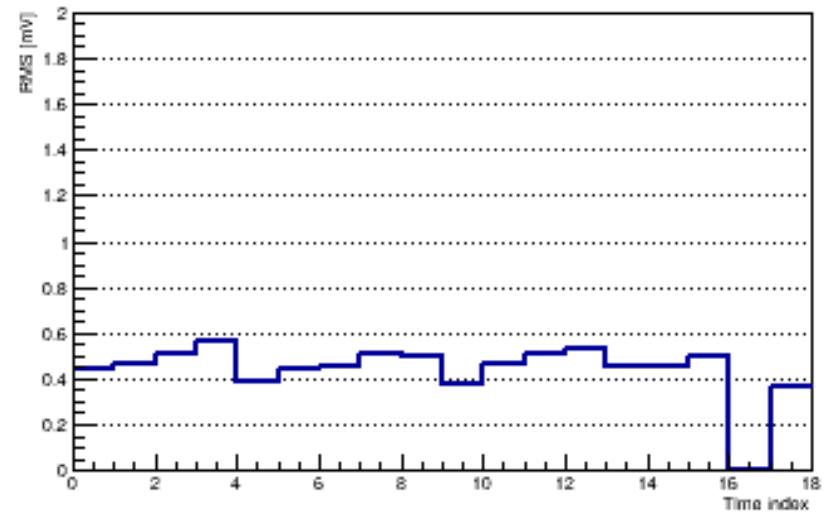


Time varying bins 61

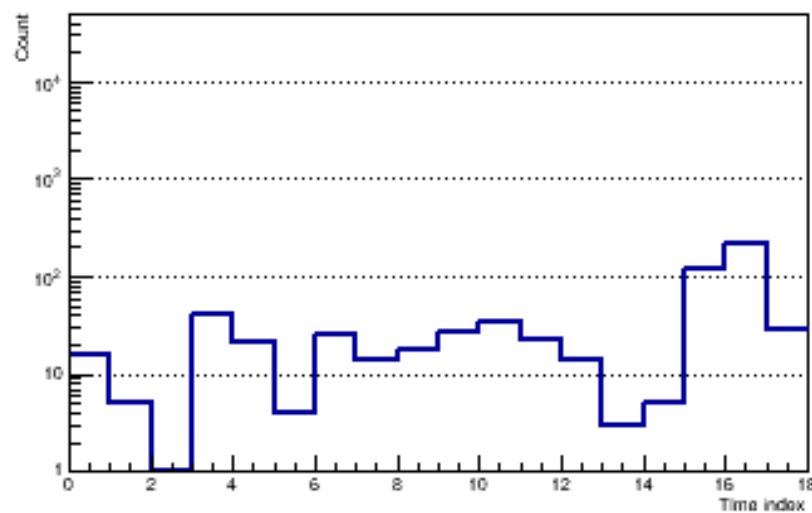
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 331



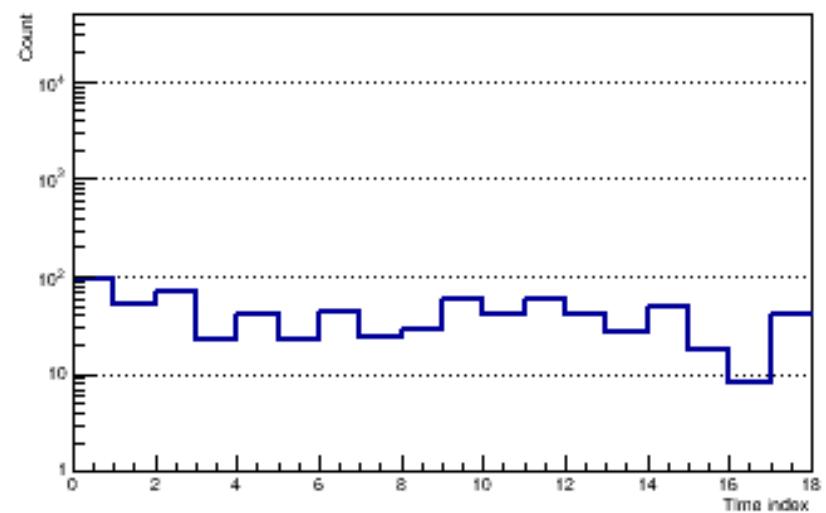
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 445



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 331

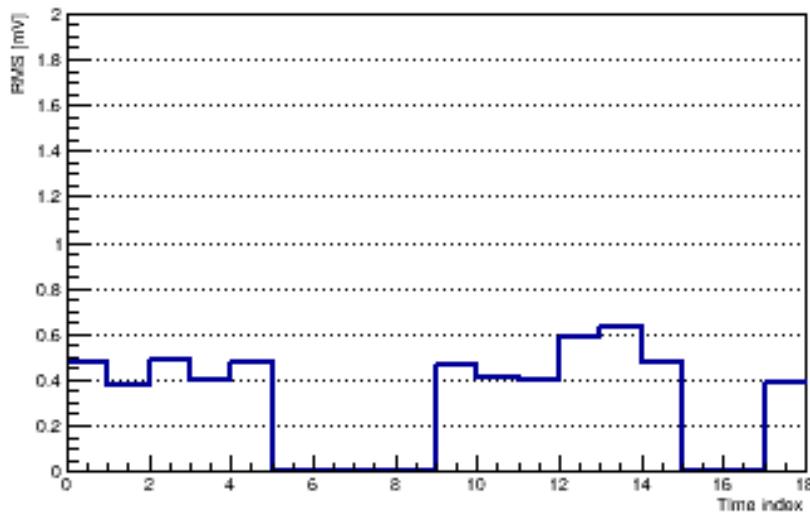


Sample count RMS for 201703b_0516 chip 2 channel 4 bin 445

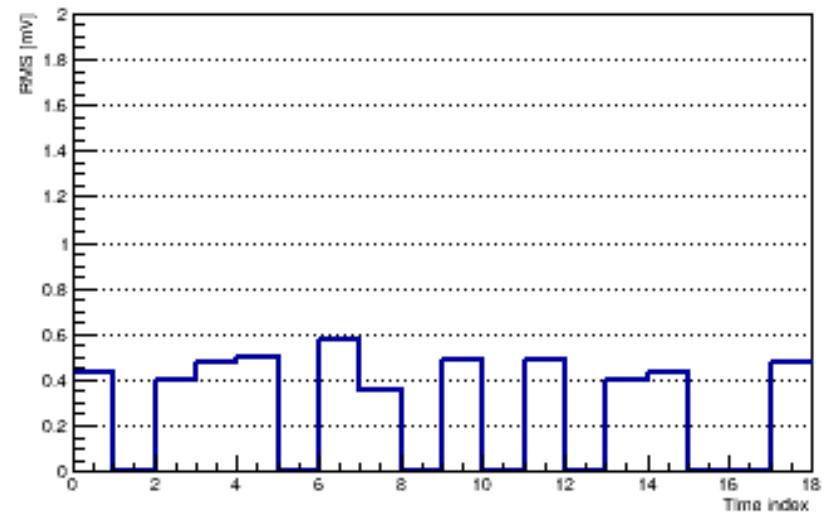


Time varying bins 62

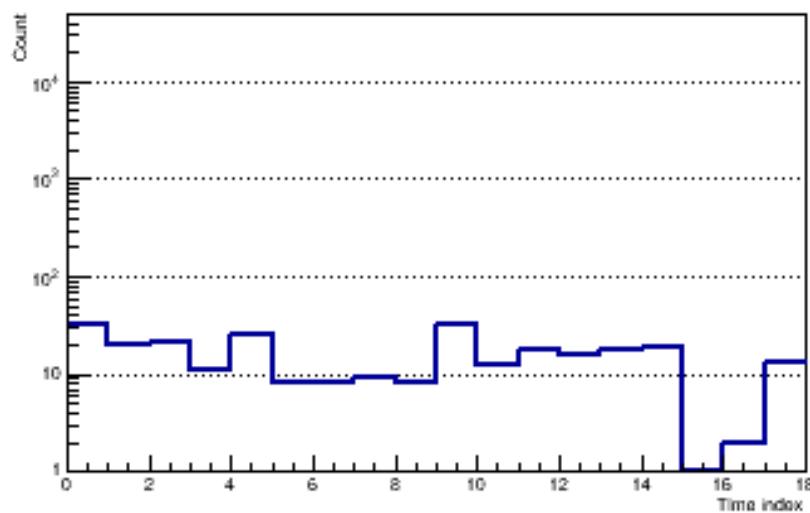
Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 446



Ultimate RMS for 201703b_0516 chip 2 channel 4 bin 509



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 446



Sample count RMS for 201703b_0516 chip 2 channel 4 bin 509

